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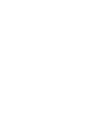
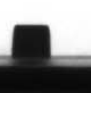
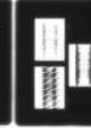
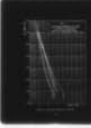
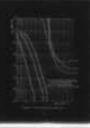
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RADC-TR-77-31
Final Technical Report
June 1977

HIGH BIT RATE DIGITAL RECORDER

Ampex Corporation



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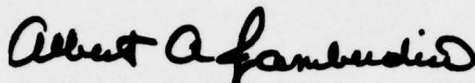
ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
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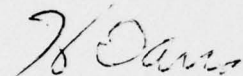
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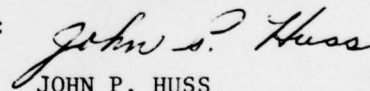
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20. ABSTRACT (Continue on reverse side if necessary and identify by block number) This report is the final report on a study program to demonstrate feasibility of recording and reproducing 240 Mb/sec digital data using magnetic tape. A transport employing two-inch wide tape and 64 track longitudinal recording heads was utilized as a feasibility model. The system included necessary electronics for operation on any 6 tracks on tape including all analog electronics, bit synchronizers, M ² Encoders and Decoders, deskew electronics and the necessary multiplexers and demultiplexers. A bit packing density of 30 Kb/in/track was used and an over all raw bit error rate, without error detection and correction, and		

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including all tape dropouts, of roughly 3×10^{-6} was achieved.

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EVALUATION

The advent of sophisticated intelligence and reconnaissance systems has resulted in the ever-increasing need to collect, process, store, and disseminate extremely high data rate and, consequently, high capacity digital information. Until recently conventional data handling techniques, through evolutionary product improvements, have been adequate to cope with this growth. However, a point has been reached where moderate improvements in the state-of-the-art are not sufficient for near term and future command and control needs for data handling.

This technology development represents a three times increase in the state-of-the-art in wide band digital recording and readout.

With the successful demonstration of machine-to-machine interchangeability, time base expansion (slow-down), and overall bit error rates of 3×10^{-6} (without error detection and correction) at these packing densities, this art is now consistent with our near and far term requirements.

Conceivably input/output rates in excess of the 240 megabits per second with total storage capacities of 2×10^{11} bits on a single reel of tape are now considered a reality.

Albert A. Jamberdino
ALBERT A. JAMBERDINO
Project Engineer

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SUMMARY

Overview

The basic objective of this program was to demonstrate the feasibility of recording a serial bit stream of 240 Megabits per second (Mb/s) on either one of the two recorders, and of reproducing the recorded magnetic tape on both recorders so that the bit error rate of the reconstituted serial bit stream does not exceed one error in 10^6 bits, both without timebase expansion, and with at least 12:1 slow-down.

These objectives were essentially fully achieved, even though the economics of the program required use of 5-year old laboratory recorder/reproducer equipment. Perhaps even more important it was clearly determined that the results were intimately dependent on the test method employed. For this reason, a substantial portion of this report is devoted to a discussion of available test methods and the corresponding dependency of the measured bit error rate.

It was particularly fortunate that the effort described here coincided with a code-comparison study sponsored by the Air Force Avionics Laboratory (Air Force Systems Command) at Wright Patterson AFB. That study revealed that a recently developed Ampex-proprietary recording code named "M²-code"* was the optimum code for the packing density to be used. This code was used in the feasibility study.

Significant Results

We believe that the program resulted in achieving a deeper understanding of the problems involved in the development of a final system capable of handling data rates in excess of 240 Mb/s. During the course of this program, specific areas investigated included the need for adequate pre-emphasis techniques to insure the capability of timebase expansion; the effect of the use of deskew electronics and parallel-to-serial converters and specific test methods on the measurement of bit error rate, and the interpretation of these measurements as applied to specific applications; the size of deskew buffers needed to insure the capability of handling two-inch wide

*See Appendix B

tape, timebase expansion, and machine-to-machine compatibility; and some limited information on the transport topology required to handle two-inch wide tape.

Future Research

Areas deserving of further investigations include the effects of crosstalk in the heads, improved pre- and post-equalization techniques, tape handling and tracking on two-inch longitudinal machines, fast start/stop characteristics using two-inch wide tape, and alternative head designs including non-standard track densities. It is also felt that some sort of tape qualification system suited for pre-selection of new tape should be developed which would be suitable for specific applications.

PREFACE

This Final Report was prepared for the Intelligence and Reconnaissance Division of the Rome Air Development Center, Griffiss Air Force Base, New York 13441, under contract No. F30602-75-C-0246 and covers the performance period of 14 May 1975 to 15 June 1976.

The technical effort was directed by Ted A. Jensen and carried out by Bill Williams and John Nakabe with significant contributions by John Konings. The program management task was assigned to Dr. Charles F. Spitzer.

The members of the program team express their sincere appreciation to Messrs. Albert A. Jamberdino and Jack D. Petruzelli of Rome Air Development Center for their initial guidance in defining and establishing the program objectives and for their consistent encouragement and suggestions in monitoring the progress of the program.

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1.0 INTRODUCTION

1.1 Background

Under an earlier program (contract No. F30602-73-C-0189) Ampex demonstrated the feasibility of 5 Mb/s operation on each of 42 tracks, on one-inch wide tape, with a bit-error rate (BER) of 10^{-6} . Economic considerations precluded complementing the full system to achieve a 200 Mb/s system bit-rate, but feasibility was demonstrated on a per-track basis, and a serial-to-parallel, parallel-to-serial pair was built to show the practicality of dividing the 200 Mb/s stream into 40 parallel channels and subsequently recombining them. Recognition of the future needs for further bandwidth increases, the need for playback with and without timebase expansion, and above all the obvious need for machine-to-machine compatibility of the recorded magnetic tape, suggested the program reported in this document. Concurrent with this effort, Ampex also was awarded a contract from Wright Patterson Air Force Base (contract No. F33615-75-C-1192) to evaluate and compare various recording codes. The results of that study established that a recently-developed, Ampex-proprietary M^2 -code was superior to both the Miller code, and the modified NRZ-codes.

1.2 Objectives

The objectives of this program included the investigation of those techniques necessary to advance the state of the art in wideband longitudinal magnetic recording to accommodate data rates in excess of 240 Mb/s. Data rates of this magnitude can only be handled on longitudinal multi-track recorders by means of splitting the data up into a large number of tracks through the use of a serial-to-parallel converter (S/P), recording these on tape and then recombining them on reproduction back into serial form through the use of a parallel-to-serial converter (P/S).

The most important performance goals were as follows:

System Data Rate (serial stream)	240 Mb/s
Per-Track Bit Rate	2 Mb/s (minimum)
Bit Error Rate (serial stream)	10^{-6}
Lineal Bit Density (per track)	25 Kb/in (minimum)

Reproduce Timebase Expansion 1:1 and 12:1 (minimum)
Machine-to-Machine Compatibility of Recorded Tape

To meet the above objectives necessitates availability of two record/reproduce systems, such that a digital bit stream could be recorded equally well on either machine and reproduced on the other. However, in accordance with economic limitations, implementation of a subgroup of tracks (5 to 10) on each machine would suffice to demonstrate feasibility, provided several subgroups of tracks would be tested by use of full-complement head assemblies, and electronics for a single subgroup on each machine. Moving the electronics from subgroup to subgroup would adequately simulate full system operation for the purposes of evaluating ultimate system feasibility. Figure 1 shows a photograph of the Ampex equipment furnished for use as the feasibility model.



Figure 1. Photograph of Feasibility Model

2.0 PROGRAM PLAN

2.1 Record/Reproduce Systems

To provide two laboratory recorder/reproducers of the latest Ampex design (FR-3000) would have entailed tying up substantial capital for nearly a year. In addition it would have involved major mechanical modification as mentioned below rendering these machines non-saleable after program completion. We therefore selected older available recorders (FR-2000) which, though not having the same capabilities as the FR-3000, would adequately serve as test vehicles for the program. Initially, a general overhaul of these two machines was required to establish performance to original FR-2000 data-sheet specifications.

To accommodate the serial bit rate of 240 Mb/s for the system, we decided on 64 tracks (60 data tracks, plus one overhead track for each group of 15 data tracks, as a part of the deskew system); the resultant per-track data rate (4 Mb/s) is well within today's technology, although the circuit design for system implementation was incomplete at the start of the program. Placed on 2-inch wide tape, the track density would thus be a mere 32 tracks per inch. This relatively conservative design ameliorates the dangers of mistracking due to tolerance build-up and assures a high degree of machine-to-machine compatibility which, it was felt, might be endangered by a much higher track density with the existing tape guiding accuracy. A mechanically redesigned transport might eliminate this as a problem. The smaller the number of tracks as used in this study, would lower the ultimate cost of full head assemblies and of a full complement of signal electronics. On the other hand, an increase in track density would ease the requirements on bits/in/track which in turn may significantly reduce the equalizer complexity and thus the per channel cost. The tradeoffs between these two approaches were not analyzed in this study.

Choice of 2-inch wide tape required Ampex to redesign the following mechanical parts (in addition to the head assemblies themselves):

1. Half-moon air guides of the Acculoop* head mount
2. All tape guides

*Trademark, Ampex Corp.

3. Capstan puck
4. Vacuum chambers
5. Reel Hold-down Assemblies

In addition it was found that the increased mass of the reels made operation of the reel servos marginal even with 14-inch diameter reels, and tests were limited to a 10.5-inch tape pack diameter. Moreover, even with 10.5-inch reels, operation above a tape speed of 120 in/s was at first uncertain. As can be seen from the nomograph of Fig. 2 this design, (solid lines) results in a lineal bit density of 33.3 Kb/in, --- well in excess of target specifications. On the other hand, a substantially more conservative design results at a tape speed of 150 in/s (dotted lines) since the lineal bit density is then only 26.7 Kb/in with resultant improvement in bit-error rate. Clearly, even this lower density is well within the 25 to 28 Kb/in specified by the program objectives.

Finally, it was felt that this choice of system design would allow for further future advances in system performance without a major redesign effort. Track density (or tape width) could be increased by perhaps as much as 50% and per-track bit rate increased to 6 Mb/s without compromising system usefulness. If feasible, such changes could well result in future system bit rates as high as 540 Mb/s. Exploration of these possibilities was not included in the program plan, however.

As stated earlier, full electronic complementation of all 64 tracks on both machines was well beyond the financial scope of the program. We therefore decided, in accordance with the Statement of Work for this contract, to test subgroups of five data tracks, plus one overhead track, i.e. a total of six tracks per subgroup. Both record/reproduce head assemblies were to have 64 tracks, so that several subgroups could be tested by merely moving the signal electronics from subgroup to subgroup, simultaneously and correspondingly on both machines. Success here would then establish system feasibility if and when full complementation were required and funded.

In the absence of signal electronics for all tracks, the recorders could not be tested at full serial data rate (240 Mb/s), of course. However, each subgroup track would still operate at 4 Mb/s, as it would do in a complete system. The performance of the subgroup of five data tracks would then have to be tested at the appropriate serial data rate, i.e. at nominally 20 Mb/s. In a fully equipped system, we would use 15 data

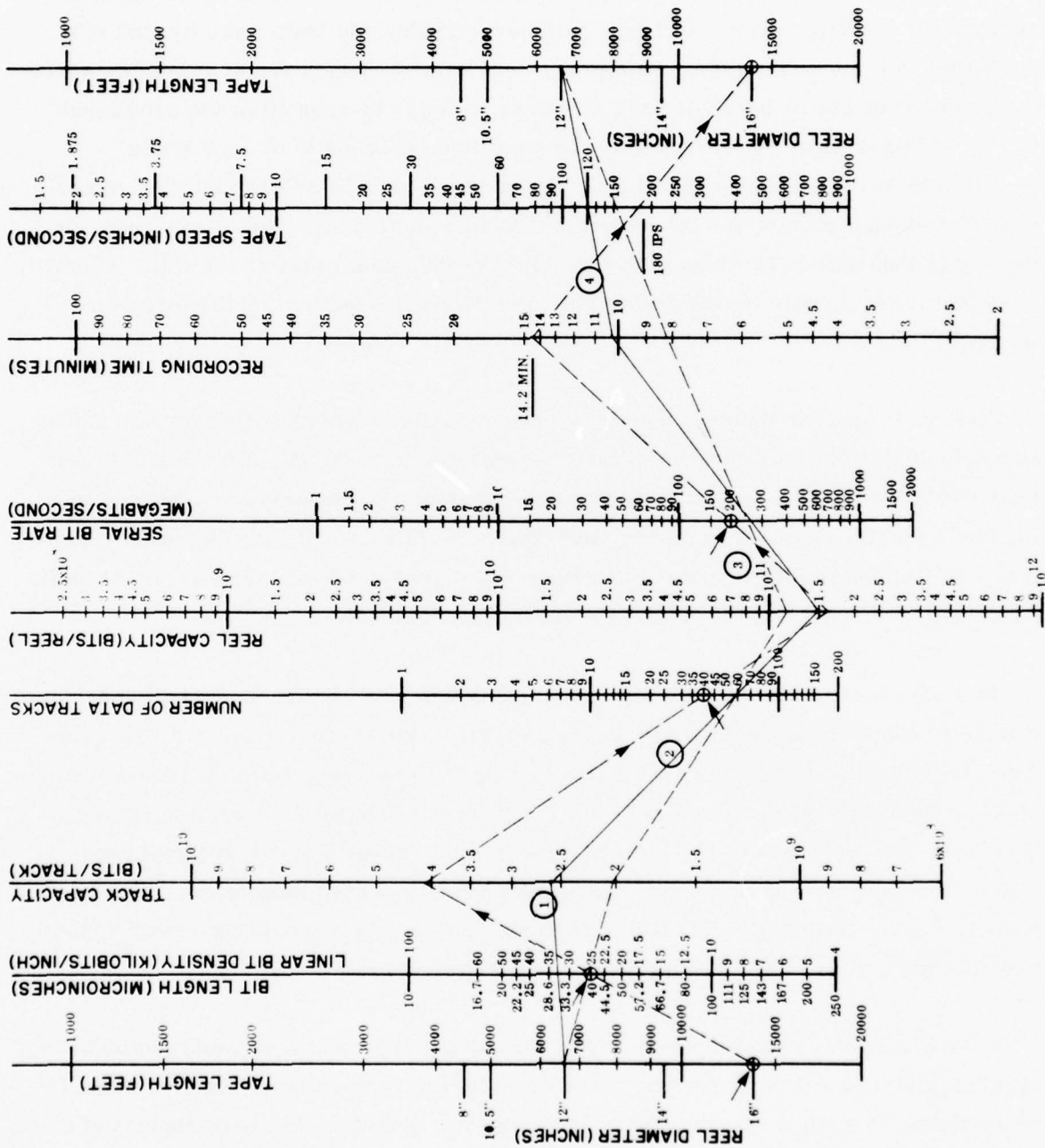


Figure 2. Design Chart for Space-Multiplexed PCM Recording

tracks plus one overhead track, per subgroup, as stated earlier. Based on our existing experience, this increase in data tracks per subgroup would offer no additional difficulties.

2.2 Test Equipment

In the absence of a definite specification for test equipment to be used, we had planned to measure BER by means of a pseudo-random word generator and comparator with a test-sequence length of 511 bits, as this has become the most generally accepted method. There remains an essential question whether error bursts should or should not be included in the count, and whether the system should or should not be allowed to resynchronize itself, in case of a sequence slip. Customarily, large bursts of errors are discounted in such tests, on the premise that they are attributable to "tape drop-outs".

The difficulty of establishing a truly valid test method was well recognized initially and was given significant attention in this program, precisely because of its truly great importance: A given system can often be made to either pass or fail the bit error rate specification, depending on the test method used.

2.3 Code Selection

The original plan was to use the well-proven Miller code to encode the data on each track just prior to the recording process (Ref. 1). Fortuitously, another division of Ampex recently developed Ampex-proprietary code for commercial broadcast television recording applications named " M^2 -code". The M^2 -code has a lowered BER, at the lineal bit densities used and under otherwise identical operating conditions (See part 4.0 of this report). It was therefore decided to provide the two test systems with M^2 logic, rather than Miller logic as was planned at the outset of the program.

3.0 RECORD/REPRODUCE SYSTEM

3.1 System Block Diagram

A block diagram of the system Ampex furnished for the feasibility study is shown in Fig. 3. On the Record side, the serial data and clock enter the Serial-to-Parallel converter (S/P). For the feasibility model, the data rate was 18 Mb/s. The bandwidth of the available reproduce amplifier was limited to 3.6 Mb/s. This was the reason for lowering the data rate to 18 Mb/s, from its 20 Mb/s nominal value. The NRZ-L data was accompanied by a synchronous 18 MHz clock. The S/P split the data into 5 lines of 3.6 Mb/s data which in turn was routed to the sync inserter. The output of the sync inserter consists of 6 lines of data each containing the proper sync information required to deskew the data on reproduction. The data are then passed through an M^2 encoder which converts the NRZ-L input data code into the M^2 code for recording in the feasibility model. The features of this code are discussed in Part 4.0 of this report. Once encoded, the information is fed to the Head Drivers which drive the six tracks on the record head.

On reproduction, the signals pass from the output of the reproduce head through pre-amplifiers and direct reproduce amplifiers with associated equalizer filters. The purpose of these filters is to equalize the channels to account for the non-uniform frequency response of the record/reproduce process. Next, the signals from each track are fed to their respective bit-synchronizer/decoder, to recover the clock from the data and to perform the bit detection process in such a manner that it reconstructs the data in M^2 form. The decoder is used to reconvert the data from M^2 to their original NRZ-L form. Once this is accomplished the data lines, with their individual clocks, enter the deskew electronics which re-align the data in proper parallel form for conversion from parallel data to serial data. This last conversion is accomplished by means of the parallel-to-serial converter (P/S). A clock multiplier is used to multiply the 3.6 MHz per-track clock to 18 MHz, at which rate the data are clocked out of the system when the reproduce speed is the same as the record speed. When 16:1 time-base expansion is used, i. e. when the reproduce speed is one sixteenth of the record speed, all data rates and clock rates are proportionately lower. (0.225 Mb/s per track, and 1.125 Mb/s for the serial output data stream.)

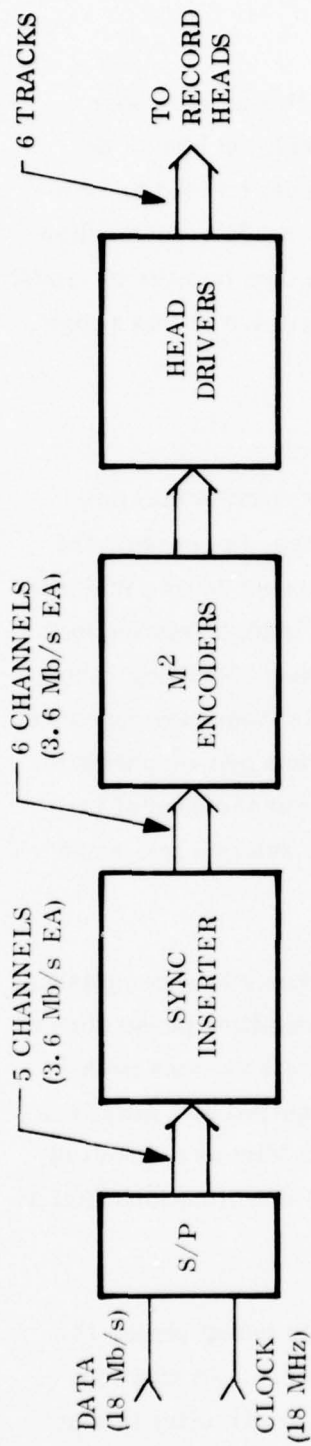


Figure 3a

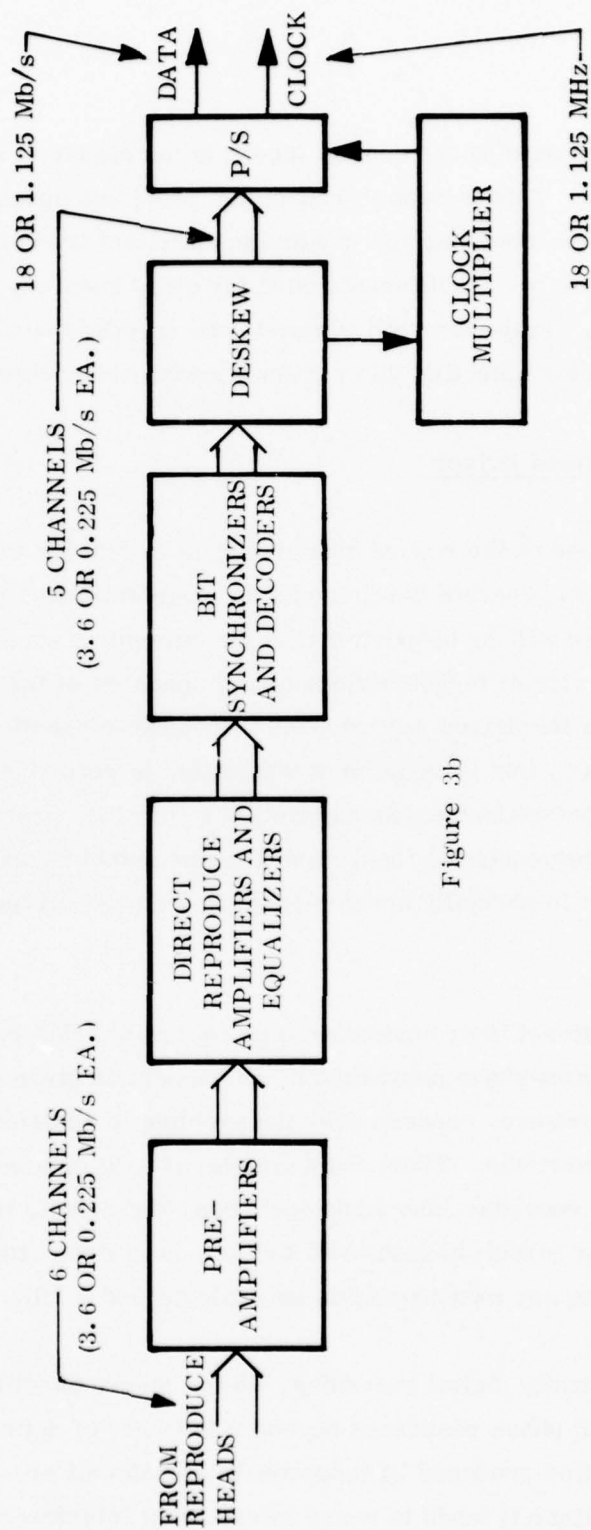


Figure 3b

Figure 3. System Block Diagram

3.2 Encoder

Prior to recording the data on tape it is necessary to encode it into some form of channel code. This is done to reduce the problems associated with the lack of dc response of the recorder and to provide sufficient transition density on tape to maintain lock in the bit-synchronizer used for clock recovery. The encoders accomplish this function. In the feasibility model, the encoders convert the data into the M^2 code. The reasons for selecting this particular code are covered in Part 4.0 of this report.

3.3 Record Head Driver

The purpose of the record head driver is to provide sufficient current into the record head to generate the flux used to magnetize the tape. Since, in general, the flux generated will be proportional to the current, a constant-current source is desirable, i. e. a circuit in which the source impedance of the driver is high relative to the impedance of the driven record head. Because in practice the head efficiency varies with frequency, that is relation of output flux to record current is frequency dependent due to core losses in the record head, it is common practice to use pre-emphasis at the higher frequencies to insure that the flux output is uniform over the band of interest. This is normally accomplished in the head driver with a suitable pre-emphasis network.

In conventional instrumentation tape recording, this pre-emphasis is accomplished with a minimum-phase network, and no concern is given to the resulting phase distortion. Furthermore, concern over the problem is restricted to what happens in the specified bandwidths. Thus, for example, if 2 dB of boost is required at 2 MHz in a conventional recorder, any additional boost that results beyond 2 MHz as a result of the particular circuit chosen to do the job, is ignored since IRIG specifications (Ref 3) do not require any measurements be made beyond 2 MHz.

In high-density digital recording, where severe bandlimiting is taking place, the amplitude and phase responses beyond 2 MHz are of definite concern. In addition, phase distortion produced by inappropriate choice of pre-emphasis circuitry is also deleterious since it tends to cause intersymbol interference which, in turn, degrades BER performance.

If the problem were limited to that of recording and reproducing at one speed, the solutions would be relatively simple. The problem of recording at high speed and reproducing at low speed causes the problem to become more complex. It becomes even more intractable when it is required that the machine record at any of the available speeds and reproduce these data at any other available speed without re-adjustment of the system.

During the course of the program, a limited amount of work was done to try and determine the optimum pre-emphasis for such a system. The results, however, leave much to be desired, and are considered to be of little use for future design efforts except to indicate that the problem appears to be more significant than was originally anticipated. The pre-emphasis network finally used consisted of a zero near band edge and a pole slightly higher in frequency. No phase compensation of the pre-emphasis network was attempted within the available time frame.

In addition to providing the current drive and pre-emphasis required for such a system, the head driver normally provides circuitry for mixing a high frequency bias greater than 3.5 times band-edge frequency with the data. This is done in conventional instrumentation recorders to compensate for the non-linearities in the B-H curve of the magnetic particles on tape. When recording digital information at relatively high data rates, the rich harmonic content of the data pulses can beat with the bias frequency and thus cause unwanted distortions in the signal prior to recording. One approach around this problem is to filter the data to reduce the harmonic content. Such filtering, however, contributes further band-limiting and phase shifts and results in additional intersymbol interference. We have found that non-bias recording eliminates this problem and thus the head drivers used for high-density digital recording at high bit rates do not provide the circuitry for mixing high frequency bias with the signal. At high data rates, BER performance proves to be better when using non-bias recording than when using bias recording. However, there remains some question as to whether performance is better or worse, when recording very low data rates if the bandwidth of the filter used to eliminate bias beats is large relative to the frequency content of the data pulses and thus has a negligible effect on the intersymbol interference in the system.

In the feasibility model used on this contract, the pre-emphasis network was chosen on the basis of obtaining the "best" eye pattern with the tape recorded at 120 in/s and

reproduced at either 120 in/s or 7.5 in/s. The network was limited to one giving one zero and one pole. Further work in the area of pre-emphasis would be required to obtain optimum results.

3.4 Pre-Amplifiers

The pre-amplifiers used in the feasibility model are mounted directly behind the reproduce head to minimize the cable capacitance between the reproduce head and the input to the pre-amplifier. This approach allows increasing the number of turns on the reproduce head to achieve greater output from the tape and at the same time maintain the resonant frequency of the reproduce head inductance and the associated cable capacitance at a frequency outside of the bandpass of interest.

3.5 Direct Reproduce Amplifier and Equalizer

The transfer function of the basic record/reproduce process of magnetic recording, i.e. between the input to the record head driver and the output of the reproduce pre-amplifier, is not flat with frequency. A typical response curve is shown in Fig. 4. In conventional analog instrumentation recorders, equalizers are used in the reproduce amplifiers to restore this response to a uniform response with frequency. This is normally accomplished in such a manner that the response for a 2 MHz recorder is within ± 3 dB from 400 Hz to 2 MHz. Since the equalization requirements for high-density digital recording are similar, but not identical to those of analog recorders, the basic equalization circuitry used generally takes the same form as that used in conventional analog recording. The exceptions have to do with the values of the components used and the reasons for these exceptions will be discussed later.

Fig. 4 also shows a typical equalizer curve for analog instrumentation recording. Fig. 5 is a simplified schematic of a typical equalizer, for analog applications.

Section (A) of the equalizer consists of an integrating amplifier to provide for equalization of the head curve in the region from "a" to "b" shown in Fig. 5. The break point at "b" is variable by means of the adjustable resistor in the feedback of section (A). The lower break point at "a" is controlled by coupling capacitors throughout the analog reproduce electronics.

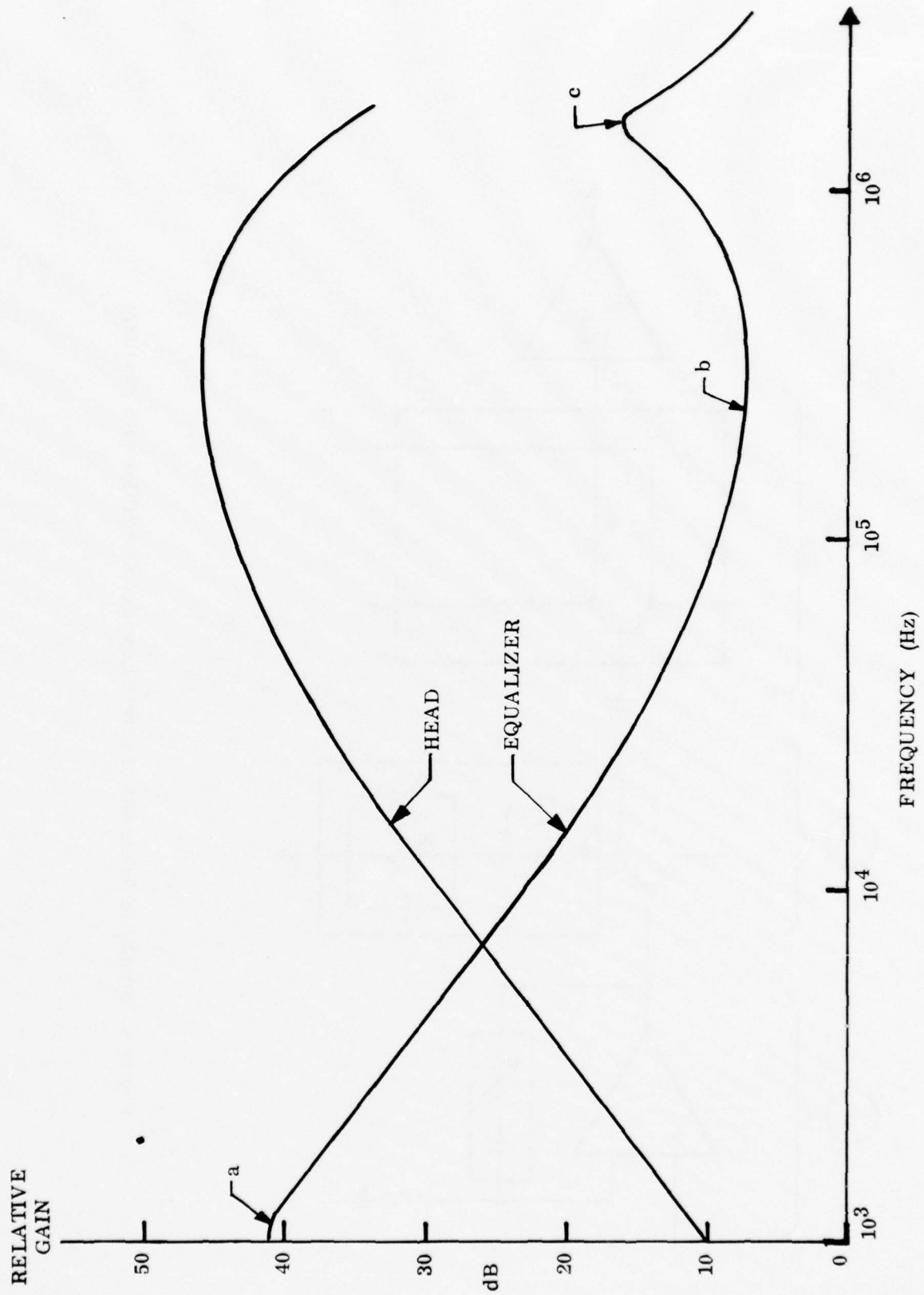


Figure 4. Typical Head and Equalizer Response

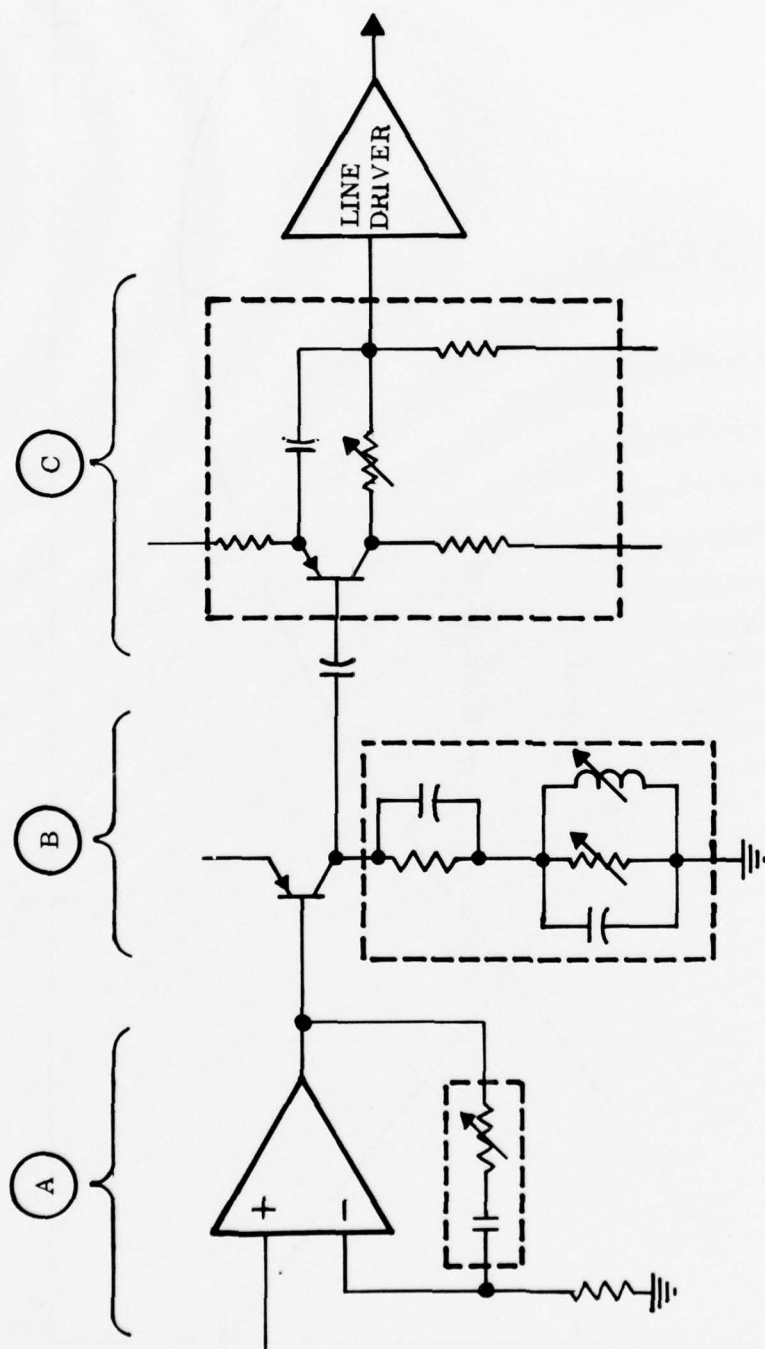


Figure 5. Simplified Schematic of Direct Reproduce Amplifier with Equalizer

Section (B) of the equalizer provides the peaking at point "c" on the curve. It consists of a current source driving the passive network shown; its output is the voltage across this passive network. The position of the peak relative to the frequency scale is controlled by varying the inductance, the amplitude of the peak by varying the resistance, of the tuned circuit. Section (C) of the equalizer is a phase compensator used to reduce phase non-linearities. The variable resistor in section (C) is used to adjust for either minimum group-delay or best pulse response, in analog recorders. In high density digital recording it aids in adjusting for the best eye pattern, and lowest BER.

Unlike analog instrumentation recording where the criterion for the various adjustments available on the equalizer is to produce as flat a frequency response as possible and as linear a phase as possible (within the capability of the circuitry available), in high density digital recording, the ultimate criterion for proper equalization adjustment is low BER. The first step is a coarse adjustment by the eye pattern improvement observed on an oscilloscope, and the second step is the reduction of the achievable BER. Adjustments for best frequency response in an analog recorder does not necessarily result in an optimal system. At low packing densities, a reduction in error rate is achievable by narrowing the bandwidth of the system to reduce the noise. At high packing densities, improvements can be made by increasing the bandwidth of the system to reduce intersymbol interference. During the course of the program it was found that the degree to which the bandwidth must change from the conventional 2 MHz bandwidth was large enough to require that the nominal values of the components should be changed from those normally used.

Furthermore, flat response with frequency proves to be undesirable when using this type of equalizer since it results in excess phase distortions, and excess noise. It was found that much better results were achievable if the high end was not boosted to the level it normally would be to achieve flat response. This reduction in boost at the high end results in less noise and lower phase distortion at the sacrifice of high frequency response, but appears to be the best compromise available for the lowest bit error rate using this circuit for equalization.

One of the goals in the original program was to use a packing density of 33 Kb/in per track at 120 in/s. This was found to be unfeasible for the existing hardware. The problem was not attributable to the basic equalization, however, but rather to

the fact that at the corresponding bit rate of 4 Mb/s per track, the basic bandwidth of the amplifier was insufficient due to stray board capacitances and other bandlimiting factors, independent of the equalization networks used. For this reason the per track data rate was lowered to 3.6 Mb/s with the resultant packing density of 30 Kb/in. The limited bandwidth of the basic amplifier (about 3.5 MHz to the 3 dB point) causes phase distortion at the high end of the band that reduces the maximum bit rate that can be passed through the system on any individual channel. It is felt that if the bandwidth of the basic amplifier were extended through re-design, performance would be improved and higher packing densities at high tape speeds could be readily accommodated.

In other on-going development programs, Ampex is evaluating alternative equalization techniques which might improve the performance of laboratory recorder/reproducer systems and at the same time keep the cost per channel reasonable.

Diode speed switching is used to switch the elements of the equalizer as a function of tape speed. This is necessary since the shape of the frequency response curve of the head varies with tape speed. In the amplifier used on this program, the circuitry is such that equalization can be accomplished at any two given tape speeds by automatic electrical switching of the speed switch on the tape transport. The particular speeds at which the amplifier may be electrically switched over are determined by plug-in cards, each of which contain the necessary passive components for equalizing the channel at a given speed.

3.6 Bit-Synchronizer Decoder

The purpose of the bit-synchronizer is to derive a clock synchronous with the data, for use in the basic bit detection process by which the signal recovered from tape is reshaped into square pulses in the M^2 -code, synchronous with the clock. The purpose of the decoder is to reconvert the reconstituted M^2 pulses and their clock to the NRZ-L code, together with a suitable synchronous clock. The Bit-Synchronizer/Decoder Ampex furnished for use in this feasibility study program is one of Ampex's latest designs for its commercial product line, and as such is a multi-speed, electrically switchable unit capable of decoding M^2 , Miller, or Bi-Phase.

The block diagram in Fig. 6 shows the basic circuit involved when used in the M^2 mode of operation. The signal from the reproduce amplifier is passed through a

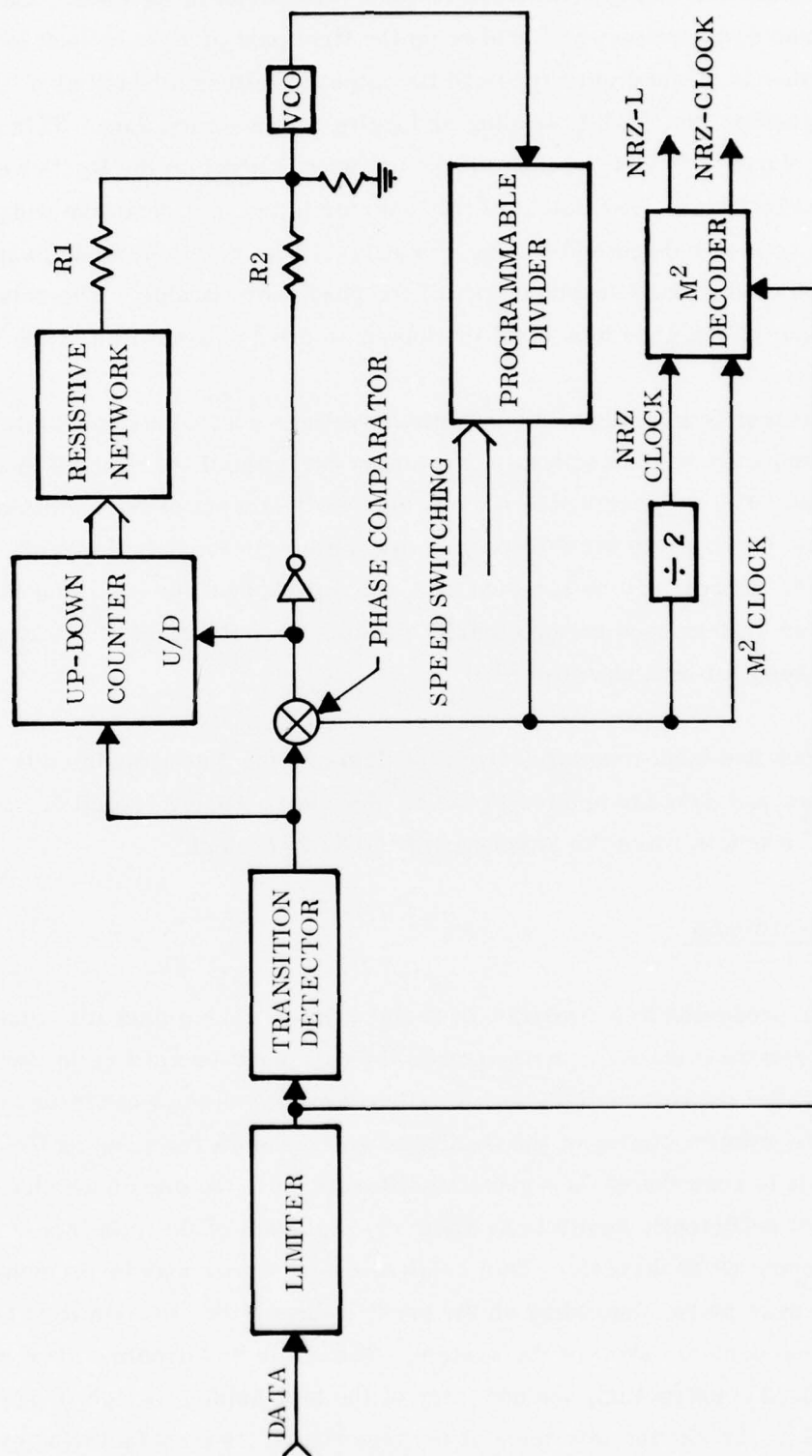


Figure 6. Block Diagram of the Bit Synchronizer/Decoder

limiter and a transition detector is used to detect transitions in the data. These are routed to a phase comparator which makes up the first part of a phase lock loop. The phase comparator is of the digital type and its output is either a "one" or a "zero" depending on whether the clock is leading or lagging the incoming data. This output is used in two places. One is the input to the up/down control on the Up/Down Counter counting data transitions. The output of this counter is fed to a resistive weighting network which acts as a digital-to-analog converter. The resultant analog signal is then mixed with the inverted second output of the phase comparator. The relative values of R1 and R2 are used to control the loop gain and the bandwidth of the loop.

The mixed output is supplied to a conventional voltage controlled oscillator (VCO). The nominal frequency of the oscillator is a binary multiple of the desired clock rate at the top speed. The programmable divider divides the output of the oscillator down to the clock rate appropriate for the speed of operation. In the actual circuit, two VCO's are used. Either may be selected by a separate speed line such that the bit rates used in the system need not be binarily related, i.e. the ratio of any two playback bit rates need not be a power of two.

Once the clock has been recovered from the data and the data translated to TTL levels, the clock and data are applied to the M^2 decoder. The $\div 2$ circuit is needed, because the M^2 clock is twice the frequency of the NRZ-L clock.

3.7 Deskew Electronics

When data is presented to a recorder in serial form of such a data rate that it is not feasible to record it directly on one track, the data must be split up by means of a serial-to-parallel converter (S/P) and distributed over a number of tracks. When this is done, the relative timing of the data between tracks on reproducing the tape, particularly if it is reproduced on a machine different from the one on which it was recorded, is not sufficiently accurate to allow re-alignment of the data in a parallel-to-serial converter (P/S) directly. This relative timing error may be as many as 25 to 100 bits, or even more, depending on the packing density per inch on each track, and the static and dynamic skew of the system. The static and dynamic skew depends in turn on the head construction, the accuracy of the tape guiding (which in practice is often limited by the slitting tolerance of the tape during its manufacturing cycle), and on any variations in electronic delays that might occur on the various tracks or

different machines. (These are generally negligible compared to the previously mentioned causes.) Some method must therefore be devised to re-align the data on the various tracks prior to any parallel-to-serial conversion, i. e. some means of deskewing the data must be used. The method used on our feasibility model has been used successfully for over 5 years, on various systems supplied by Ampex.

In order to deskew the data, there must be some information recorded on the tape that can be used as a reference to determine precisely how the data should be re-aligned. This is accomplished by framing the data by inserting a sync word into each channel. The method of sync insertion used can best be described by reference to Fig. 7.

This figure illustrates the process for a condition where 5 data channels are used, but can be extended to any number of data channels desired. The sync word used is 16 bits in length. In the figure the data are arbitrarily blocked into 16-bit word lengths as they enter the recorder system. The sync word is distributed to all channels as shown in the figure. Each time a sync word is inserted in a particular channel, it is substituted for the data that were present on that channel. The data, in turn, are temporarily stored in the master channel. This process is continued as shown in the diagram until each channel, including the master channel, contains a sync word every 256 bits.

Once the sync word has been inserted into the data streams in the manner shown in Fig. 7, it is possible, on reproducing the tape, to hold this information in storage buffers (one for each track) to re-align the data to their time-relation prior to recording and to release them simultaneously under control of an output clock common to all channels. In the feasibility model, the clock used for this purpose is generated by the bit synchronizer used on the master channel. This is accomplished in the following manner:

Fig. 8 is a simplified schematic of the deskew logic, showing the master channel and a single slave channel. (The data channels are referred to as slave channels since the outputs of these channels are controlled by the master channel clock.)

Each channel in the system contains a sync detector used to detect the sync word that has been inserted into the data stream, a presettable binary counter used to

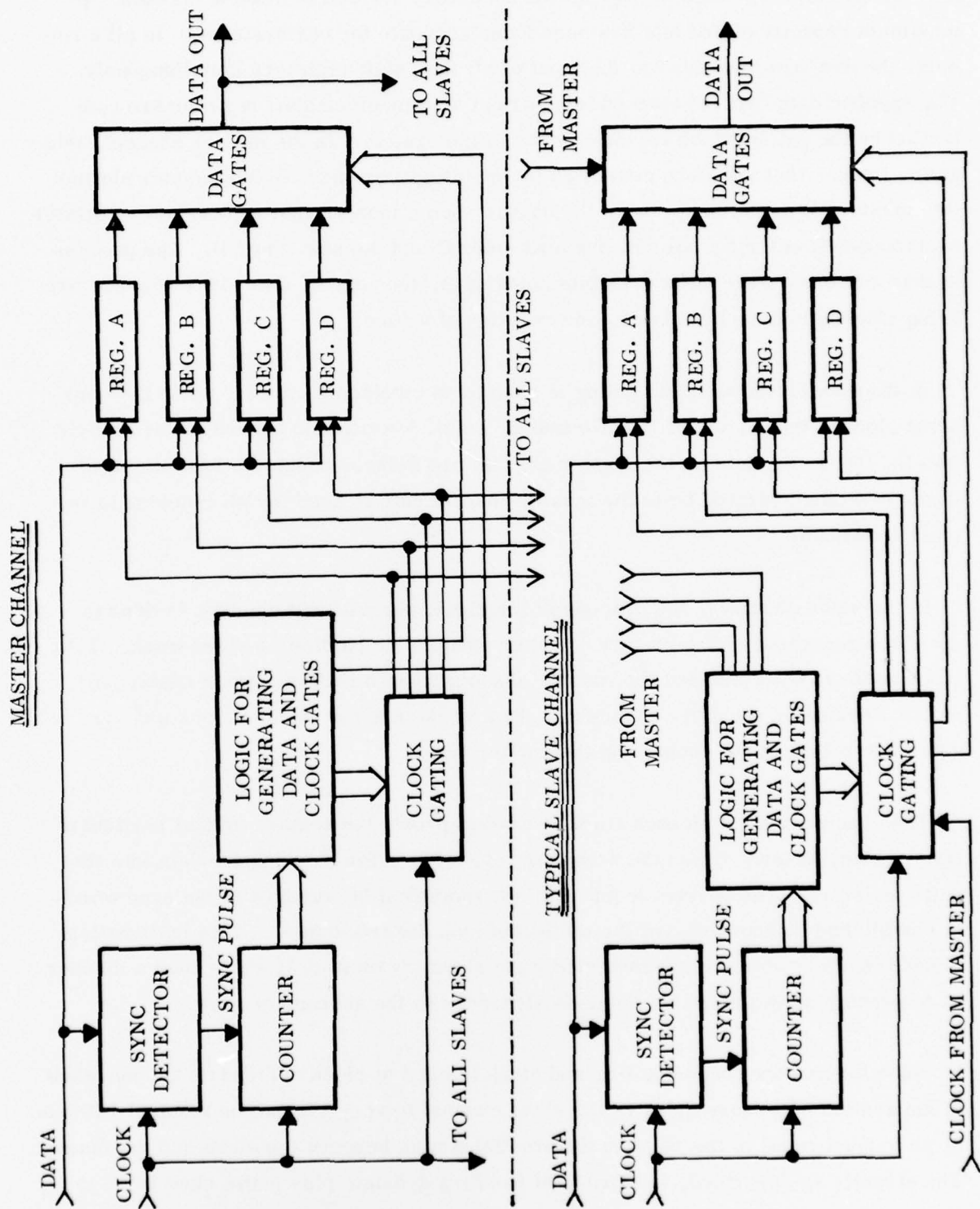


Figure 8. Simplified Schematic of Deskew Logic

generate proper gating information relative to the sync word on each channel, and four 64-bit shift registers to provide the necessary storage to deskew the data. (A maximum capacity of ± 64 bits has been found adequate for our systems.) In all channels, the data are presented to the input of all four shift registers simultaneously. The specific data that get clocked into, or out of, any given shift register are controlled by the gating of the various clocks in the system. In the master channel, this gating is such that the clock generated by the bit synchronizer on the master channel (the master channel clock) clocks the data in such a manner that 64 bits enter register A, the next 64 enter register B, the next enter C and the next enter D. The process is then continued with the next 64 bits entering A, the next B, etc. Thus the data are being clocked into each register, one register at a time.

In the master channel, the gating is such as to clock data out of C while they are being clocked into A, out of D while into B, out of A while into C, and out of B while into D. Thus, the data on the master channel are delayed precisely 128 bits at all times (the clock derived from the master channel data is used for all clocking in the master channel).

In the slave channels, the process is identical, but all input clocking is done by the clock generated by the bit synchronizer used on the particular slave track. This clock controls the gates and the counter associated with that particular track. All output clocking on the slave channels is done by the master channel clock and the gates controlled by the counter on the master track.

The sync word used on each track is used to preset the counter on that particular track which, in turn, times the necessary clock gates for clocking the data into the shift registers. The correct location of any individual bit relative to the sync word is established by knowledge of the method of sync insertion used. This information is used by the counters and associated logic circuitry on each track in such a manner as to provide an exact 128 bit delay on all tracks in the absence of skew.

Since the master channel gating and clock is used to clock out all tracks, any skew in the system will cause delay in the slave channel to vary around the nominal 128 bits by an amount equal to the relative differential timing between the slave and the master. The circuit, as described, is capable of handling dynamic plus static skew of up to plus or minus 64 bits.

It should be noted that this method of deskewing results in removing all relative timing errors between the data tracks and the master track, but does not remove any timing perturbations on the master track caused by timebase error or flutter in the recorder. It simply assures that all tracks remain synchronous with the master channel clock even in the presence of timebase instability caused by flutter on the master track. The disadvantage of this arrangement is discussed in Section 3.8.

In addition to deskewing the data in the manner just described, the deskew electronics returns the data temporarily stored on the master track during the sync insertion process, back to their respective original slave channels. Thus the output of the deskew electronics consists of 5 lines containing data identical to the data presented at the input to the sync inserter (assuming no bit errors).

Also contained within the deskew circuitry, but not shown on the simplified schematic, are the necessary circuits to reduce the probability of the sync detector indicating the presence of a sync word erroneously because it happened to appear in the data. This is accomplished by means of a gating system which provides a window for the sync detector. Once a sync word is detected, this window is closed until 4 bits prior to the time the next sync word is expected. In this manner, should the data happen to contain 16-bit sequences identical to that used in the sync word, the sync detector will ignore it.

If, by chance, the first sync word detected is false, i.e. it is actually a 16 bit data sequence identical with the sync word, the window will close and miss the actual sync word. However, during the next 256 bit frame, the data will, in all probability, change, and the sync detector will detect a different 16 bit sequence. When this happens, the window will open and all data will be passed through it once more until it detects a proper sync word which will then lock up the system.

The method used for sync insertion and deskewing is such that no preamble is required on the tape; the recorder may be started anywhere in a reel of tape and the system will lock up and deskew the data properly.

The choice of buffer size which would accommodate plus or minus 64 bits of static plus dynamic skew was based on measurements of actual skew on a one inch machine some years ago when packing densities were lower than those currently being investi-

gated. With the higher packing densities and the wider tape being considered, the size of the buffers will probably need to be increased if full consideration is to be given to the problems of machine-to-machine compatibility, particularly between the airborne recorder and a ground based reproducer which might employ different tape path topologies. In anticipation of this expectation, Ampex has currently under design a deskew system capable of handling larger amounts of skew.

In addition, the new deskew electronics will be able to provide for full timebase correction and will thus eliminate problems caused by residual clock timebase instabilities on the master channel. The program scope did not allow for incorporation of this new deskew system into the feasibility model.

3.8 Serial-to-Parallel and Parallel-to-Serial Converters

The Serial-to-Parallel Converter (S/P) is conventional in design and need not be discussed here.

The Parallel-to-Serial Converter (P/S) deserves discussion only in that it may be a partial contributor to the measured BER, to explain the reasons for this conclusion, and to propose a solution to this problem. A simplified schematic of the P/S is shown in Fig. 9. The most critical portion of the circuit is related to the development of the high-frequency clock. In the design, as implemented, this high-frequency clock is developed by multiplying the master channel clock frequency by a factor of five by means of a phase-lock loop. (The frequency-multiplying factor is determined by the number of parallel channels, per serial output channel.)

The master channel clock contains timebase errors caused by flutter in the recorder. It is important that the bit synchronizer should follow this flutter to prevent deterioration of the basic bit detection process. In so doing, the frequency modulation of the data, caused by the flutter, is transferred directly to frequency modulation of the clock developed by the bit synchronizer. Thus one can consider the master channel clock as a frequency modulated square wave. The multiplication of a frequency modulated waveform by a phase-lock loop (or by any other means) results in a multiplication of the modulation index by the same factor. That is, it multiplies the degree of modulation.

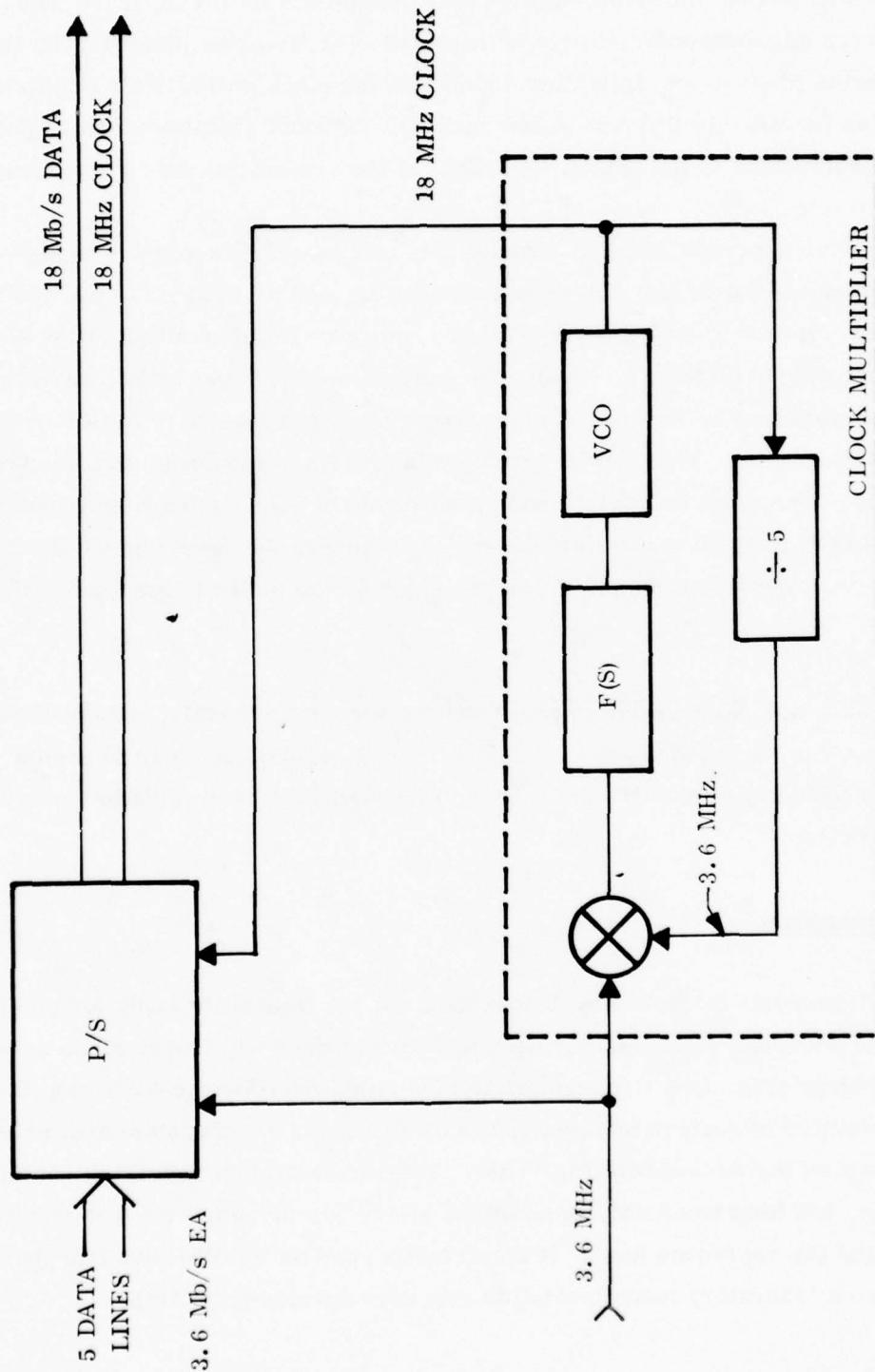


Figure 9. Parallel to Serial Converter

In the time domain the problem may be described as follows: If the jitter, i.e. the timebase error, on the master clock is one microsecond, prior to multiplication by five, it will still be one microsecond after multiplication. However, if the period of the clock is ten microseconds prior to multiplication by five, the jitter will be 10% of the clock period prior to multiplication and 50% of the clock period after multiplication. Such an increase in jitter as a percentage of the clock frequency can be deleterious to the reclocking of the data at the output of the system and cause bit errors.

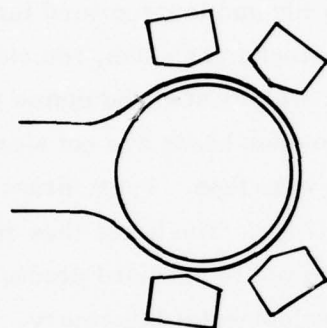
An alternative approach which eliminates this problem is to use a stable high-frequency clock, derived from a crystal for example, and to divide it to provide the low-frequency clock. When this is done, the problem of flutter multiplication disappears. In order to do this, however, the problem now becomes one of providing the proper phase relationship between the low-frequency clock developed in this manner and the data from tape. This can be accomplished by timebase correcting the system. Such timebase correction is feasible and breadboards of such systems have been developed at Ampex independent of this contract. However, the development of the timebase corrector was not completed soon enough for inclusion in the feasibility hardware.

In the future, and particularly where it will be necessary that the ratio of the high-frequency clock to the low-frequency clock be high, e.g. 60:1, the use of such a timebase corrected system will eliminate the need for clock multiplication and its inherent weakness.

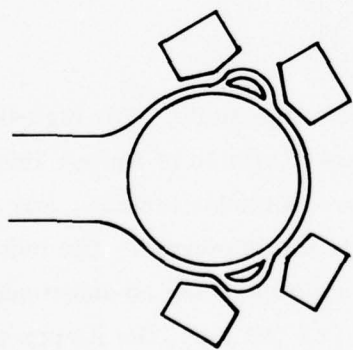
3.9 Tape Transports

The tape transports furnished by Ampex used for the feasibility study (originally Ampex Model FR-2000) were initially designed for one-inch wide tape, and a zero loop tape topology (Fig. 10a). In addition to modifying them for two-inch wide tape, they were modified to replace the zero loop with the latest drive system available at Ampex, known as the Accu-Loop (Fig. 10B). This drive system results in excellent tape handling, low head wear and, in addition, allows for mounting the pre-amplifiers directly behind the reproduce head. It is currently used on the FR-3000 transport, the most recent laboratory instrumentation recorder developed by Ampex.

Some difficulties were encountered early in the program with the capstan and reel servos available on the machine when the system was required to operate with 2-inch



ZERO LOOP
(a)



ACCULOOP
(b)

Figure 10. Schematic Representations of Zero Loop and Acculoop
Tape Path Topologies

wide tape, but these were overcome through modification of the servos. Similarly, some problems involved the design of a vacuum chamber ultimately suitable for two-inch wide tape. In any final system, the transport used would be one designed initially to handle two-inch wide tape and these problems would not occur.

3.10 Heads

The heads used on the system were two inches wide and incorporated the full set of 64 tracks, as they would in the final system (32 tracks per stack, interlaced format). Since the standard drawings for 32 track heads per inch existed and define track width, spacing, manufacturing techniques, etc., these two-inch heads are not significantly different from those built in the past, for one-inch wide tape. These drawings were marked up and delivered to our manufacturing facilities. The heads thus represent a quality commensurate with that which would be achieved in standard production today as opposed to that which might be achieved in a developmental laboratory. It was felt that this was important in order to assure that data taken during the study be as close as possible to those which might be achievable with production heads.

3.11 Tape

Two-inch wide tape was used during the course of the study. For high-density digital recording applications, one of the best tapes available is Ampex 799. This tape is pre-tested for dropouts, but only in the one-inch wide format. For this program, two inch wide Ampex 799 tape was specially manufactured. The industry standards for high resolution wideband tape allow an average of ten 10-microsecond dropouts per track in every 100 ft. segment of tape. For 799 tape, the Ampex standard for average dropout count is reduced to one in a 100 ft. segment with an allowable duration of only one microsecond. Every single reel of 799 is tested from end-to-end. Every other track (14 tracks) of a 28 track configuration, one inch wide, is tested. It must be emphatically stated, however, that even this quality standard does not provide protection against significant numbers of multi-bit tape dropouts, when the tape is used in a high bit-density application. Currently no test system is available for two-inch wide tape to assure 799 quality. To provide a high probability of obtaining suitable tape for this program, two-inch width tape was cut from various webs, along with one-inch tape cut from the same webs. The two-inch tape eventually supplied came from webs where the one-inch tape supplied from the same web met the specifi-

cation for 799. Even with this precaution, some of the two-inch tape received showed a large number of dropouts once the system was operating in its final configuration. However, this tape was used a great deal in establishing system operation and was probably damaged by poor tape handling of the transport early in the program when tape handling was still a problem.

Use of this poor tape proved useful in uncovering variations in bit error rate as a function of system configuration and test methods, however, (see Parts 7.0 and 8.0 of this report) good tape was used for all final testing.

4.0 CODE SELECTION

One of the most important factors in successfully developing a system with low BER at packing densities commensurate with reasonable record times, is the selection of a suitable channel code. The incoming data are virtually always presented in the form of an NRZ-L code with a synchronous clock. Because of the dc content that can exist in this code, depending on the pattern of "ones" and "zeroes" presented to the particular track, and because the basic reproduce process inherently lacks the capability of recovering dc from the tape, it is necessary to encode the data in some form of channel code prior to recording. The primary purpose for such encoding is to reduce or eliminate the need for dc response in the recorder. A secondary purpose is to provide sufficient transition densities in the data stream to allow clock recovery by means of a phase-lock loop. As a result of previous studies (Ref: 2) which consisted of comparing the various codes available at the present time, we selected the recently-developed Ampex-proprietary M^2 -code.

The M^2 -code described in Appendix B of this report, is a modification of the Miller Code such as to make the code dc free. This results in a code that is virtually free of pattern sensitivity. Figures 11, 12, and 13 illustrate the degree of improvement possible when using this code at high packing densities as compared to other codes. The significance of these plots is described in the next paragraph. A fuller discussion of comparative code performances is found in Ref. 2.

4.1 Record Margin

The concept of record margin is as follows: It is known that the bit error rate will suffer if the signal-to-noise ratio of the system is degraded. A simple method of degrading this ratio is to record the signal at a lower level. The record level is therefore reduced and the gain of the reproduce amplifier increased to give the same nominal output as prior to reduction in record level. The resulting reduction in signal-to-noise ratio at the output of the system which results in a given BER is called the record margin for that BER.

Using this concept, it is possible to compare two codes and state that for a desired BER the code allowing the greater record margin is superior by a relative amount expressed in decibels. The limitations of this method are discussed in detail in Ref. 2.

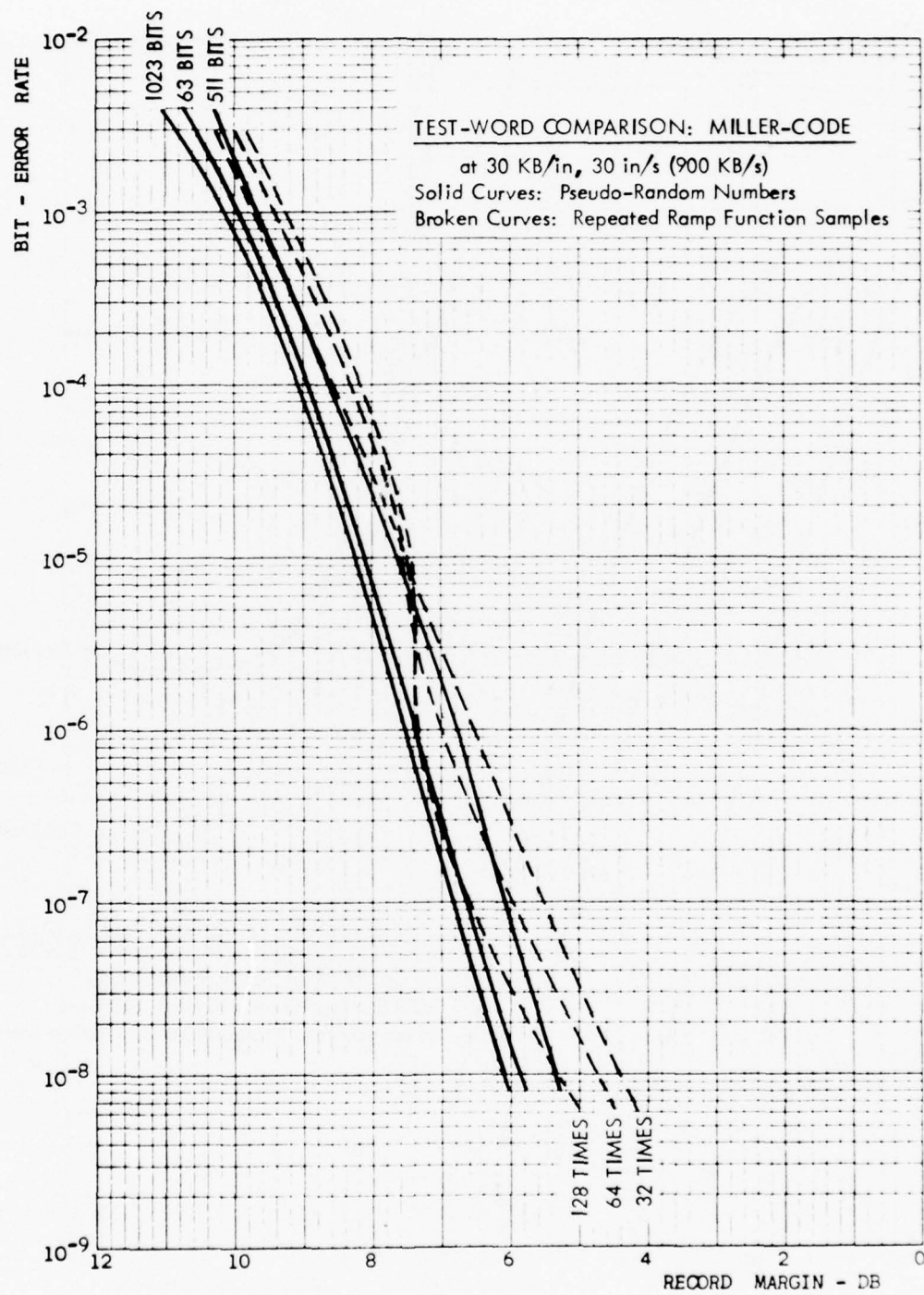


Figure 11. Test Word Comparison: Miller Code

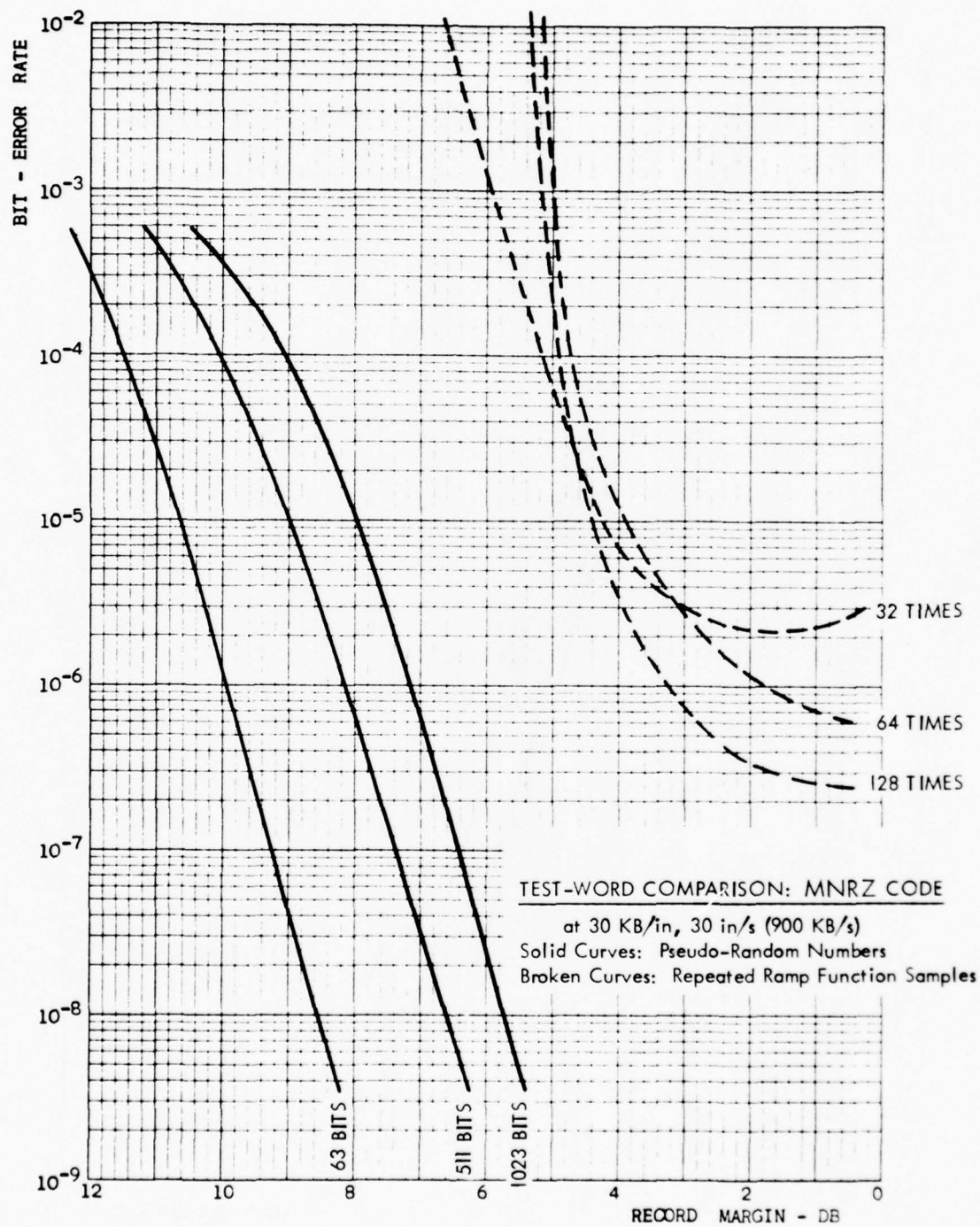


Figure 12. Test Word Comparison: MNRZ Code

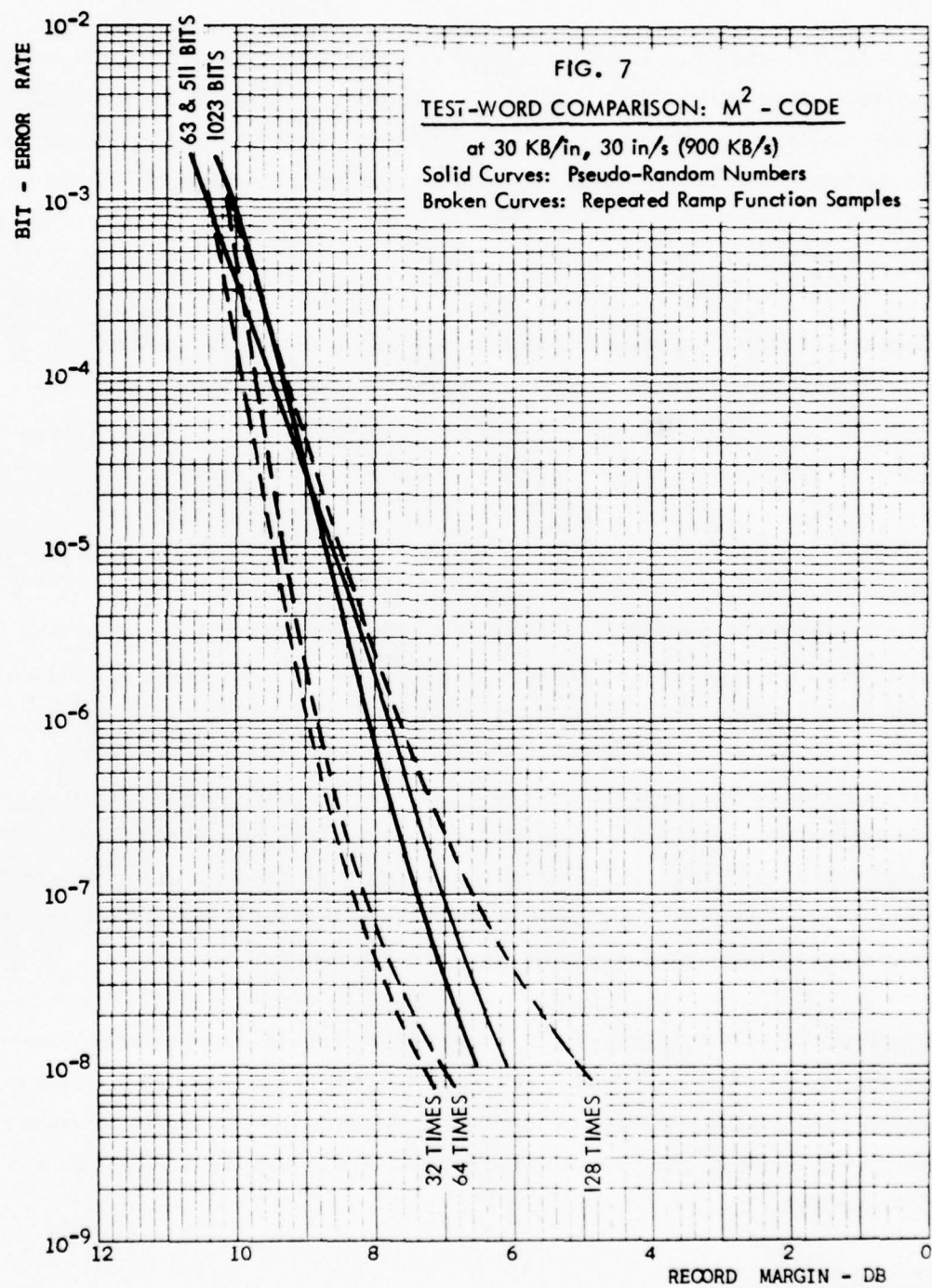


Figure 13. Test Word Comparison: M^2 Code

Since BER is a function of the pattern recorded in pattern sensitive codes, it is possible to measure the degree of pattern sensitivity of a code in a similar manner.

Figures 11, 12, and 13 are results of tests of this type for three different codes. The codes used were Miller, M^2 , and MNRZ. MNRZ is a modified form of NRZ wherein the encoding process consists of inserting an eighth bit for every seven data bits with the inserted bit being the logical complement of the seventh bit. This technique assures that there is at least one transition every eight bits. Details of the code are described in Ref. 2.

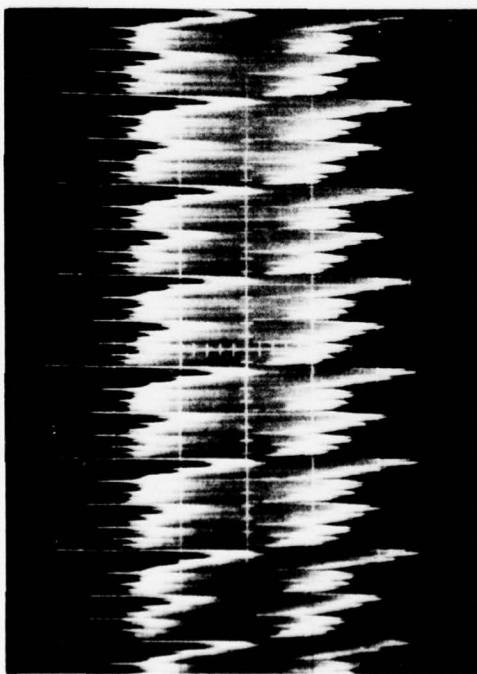
All data used in the plots shown were obtained on a one-inch 14 track system at 30 in/s and a packing density of 30 Kb/in. Six different test patterns were used. The details of the test patterns and measurement techniques are covered in Ref. 2 and are partially described in Part 8.0 and Appendix A of this report.

The plots show clearly two significant factors. The first is that the MNRZ code is pattern sensitive. This can be seen by virtue of the fact that for a BER of 10^{-6} the record margin is highly dependent on the pattern used for testing. The second is that for the worst-case pattern and an error rate of 10^{-6} the M^2 code is about 1 dB superior to the Miller code. The one dB differential between the Miller code and the M^2 code may at first not seem like a meaningful achievement, but it does, in fact, represent an order of magnitude difference in BER. Furthermore, additional tests on this one-inch machine show that at a slightly higher packing density (40 Kb/in) the worst-case record margin for M^2 was approximately 3 dB for a bit error rate of 10^{-6} , whereas for these patterns, neither Miller code nor the MNRZ code were able to recover these patterns with an error rate of better than 10^{-1} .

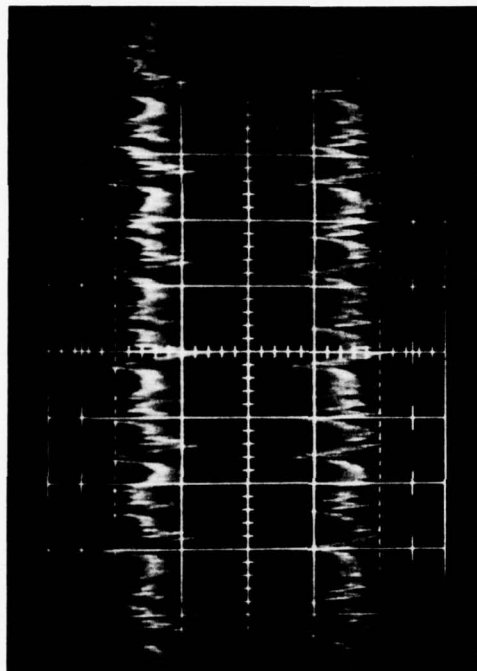
To illustrate the effectiveness of a dc free code such as M^2 in eliminating baseline drift due to lack of dc response in the basic reproduce process, Fig. 14 shows oscilloscope photos of the envelope of the data at the output of the direct reproduce amplifier (prior to use of "dc restoration") for the three codes at 30 Kb/in for the worst-case pattern.

4.2 Selection of M^2 Code

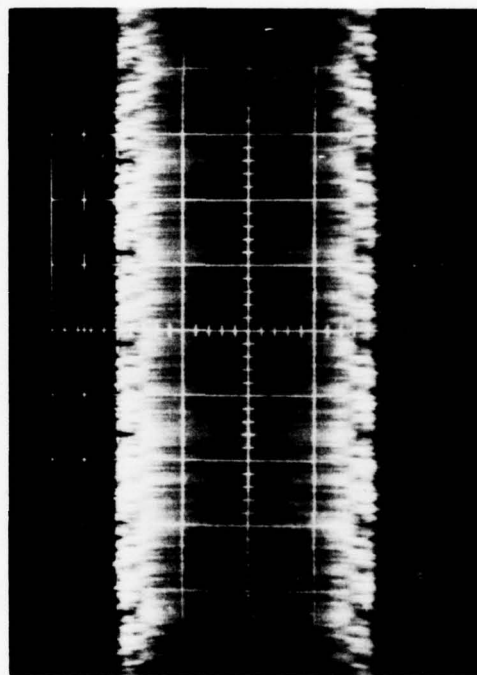
Because of the measured superiority of the M^2 code over the other codes currently



MN RZ



Miller



M^2

Figure 14. Oscilloscope Traces for Three Codes at Reproduce Amplifier Output

available, it was chosen as the channel code for use on this program. Differentials between the BER achieved on this program and the BER achieved on the one inch machine used in Ref. 2. are discussed in section 8.0 of this report and are not attributed to the choice of code.

5.0 PROBLEMS

In addition to those problems covered in particular sections of this report, e.g. reproduce amplifier bandwidth (section 3.5), it is necessary to examine those problems which precluded the packing density from exceeding 30 Kb/in and to review why the BER ultimately measured did not quite reach the target goal of 10^{-6} .

5.1 Original Plan

We originally planned to test the systems at 4 Mb/s per-track bit-rate and with a 64-track head which would support a through-put rate of 240 Mb/s on 60 tracks leaving 4 tracks for overhead to be used for deskewing. At 120 in/s the resulting lineal packing density would then be 33.3 Kb/in (see Fig. 2.1). This was not accomplished and the packing density had to be lowered to 30 Kb/in for reasons, some of which have already been discussed. There are other reasons worthy of consideration, however.

5.2 Reasons for Measured BER at 30 Kb/in/track

Figure 3.11 shows that at 30 Kb/in the record margin for a BER of 10^{-6} is about 8 dB. However, these results were obtained on a machine with a 14-track, one-inch head, i.e. with a track width of 0.050 inch. The track width for the two-inch, 64-track system used for the planned 240 Mb/s program should be about 0.020 in. Measurements showed the actual track width to be only 0.016 in due to improper alignment of the two halves of the ferrite core, where the gap of the head is formed.

If it is assumed that the pre-amplifier is perfect and neither it nor the real part of the head impedance contributes noise to the system, the loss in signal-to-noise ratio (in decibels) due to track width reduction is given by the expression $10 \log R$, where R is the ratio of the track widths. In this case the resultant loss between the one-inch machine and the two-inch machine should have been about 5 dB. An additional reduction in effective track width will occur if the above-mentioned core, misalignment exists on both the record head and the reproduce head, but does not match in position. The result will be mistracking. If it is assumed that all of the noise in the system is generated by the thermal noise in the head in combination with the noise in the pre-amplifier, the loss would be 10 dB. In actual practice, the noise

generated by the head itself varies as a function of frequency. In some parts of the spectrum the tape noise (particulate noise) dominates, whereas in other parts, electronic noise (including thermal noise of the head) dominates.

Furthermore, errors are caused by a combination of noise and intersymbol-interference. Intersymbol-interference, in turn, is caused by a lack of high-end-frequency response. The two-inch system lacked the necessary high-end response relative to the one-inch system for two reasons: First, the bandwidth of the reproduce amplifier was insufficient as was previously discussed, (Sec. 3.5) and second, the short-wavelength response on the two-inch head was slightly lower than that achieved on the one-inch head, due to manufacturing tolerances. Furthermore, a reduction in short-wavelength response causes both decreased S/N and increased phase distortion due to the difference in equalization required. Phase distortion, in turn, causes an increase in intersymbol interference. Unfortunately, it is not possible to identify the cause of a given error as being either due to noise, or intersymbol interference, since the effects are additive. It is only possible to state that the combined effects of the narrower track width, the limit on frequency response of the reproduce amplifier, and the reduction in short wavelength response, could all, in combination reduce by a significant amount the record margin for 30 Kb/in at a BER of 10^{-6} .

Experience indicates that if a system operates with zero record margin at 30 Kb/in with a BER of about 10^{-6} (which was the case for the system as finally configured), increasing the packing density to 33 Kb/in will result in a degradation of the BER by two order of magnitudes, unless the record margin at the lower packing density can be improved by about 2 dB.

Other differences between the two systems could also account for the increase in BER on the two inch system. These include:

- a) The one-inch system was tested on a single track with one channel of electronics and thus avoids electronics crosstalk in the trays and through common power supplies such as were used in the two-inch system.
- b) Low-frequency noise was apparent in the two-inch feasibility model and was attributed to system ground loops. Although some improvements were made during the course of the study, it is felt that further improvements are possible.

6.0 TEST PLAN

Originally we planned to measure BER on serial data stream only, on three separate groups of six tracks each (five data tracks plus one master track for deskew in each group). During the debugging phase of the program, it was noticed that there appeared to be an excessively large variation in BER as a function of machine configuration and/or test equipment. It was felt important to investigate the cause of this observation and the test plan was revised to include BER testing of individual tracks both with and without deskew electronics as well as of the serial data stream.

Further testing revealed much of this differential was due to variations of the type of test equipment and the mode in which it was operated. The details and the reasons for it are covered in Part 8.0 of this report.

The test plan which eventually evolved was:

- a) All tests would be run with the Tautron test equipment (discussed in Sec. 8.2) since it was the only equipment capable of handling the serial rate.
- b) All tests, except the final tests on the three sub grouping of tracks, would be duplicated in two modes of test equipment operation, one known as a "Low Burst" mode and the other a "High Burst" mode. The reasons for this decision will be reviewed in Parts 7.0 and 8.0 of this report.
- c) All tests would be made at 120 in/s record speed on machine A and at 120 in/s and 7-1/2 in/s reproduce speed on both machine A and machine B. This experiment would test for slow-down capability and machine-to-machine compatibility.
- d) All tests would be run using a 511-bit pseudo-random sequence. Although in some codes, pattern sensitivities exist such as to make a large differential in BER as a function of the pattern used, preliminary tests on this equipment plus extensive tests on a previous program (Ref 2.) revealed that the M^2 code displayed negligible pattern sensitivity. (See Part 4.0 of this report for a review of code comparisons.
- e) In all tests, all errors would be counted including all burst errors due to tape defects. This decision was made since burst errors may be caused by factors

other than tape defects (see Part 8.0 for other causes), and it is not possible to identify whether or not a particular burst was due to a tape defect or one of these other causes. This decision is particularly noteworthy, because it has become accepted practice to exclude large error bursts from the count, on the presumption that such bursts are due to tape defects, rather than the recorder/reproducer as such.

7.0 TEST RESULTS

Table 1 is a tabulation of the final data taken on the serial data stream, for three separate groups of six tracks each. The mean BER of all of these tests, which includes all burst errors, is 3.2×10^{-6} . The track groupings were chosen in the following manner:

Group #1 consisted of tracks 22, 24, 29, 31, 38, and 40. These tracks were chosen at random and covered about the center half-inch of tape. Group #1 was used for all of the BER measurements of individual tracks as well as for the final BER measurement on the serial data stream. The tracks are "paired" (e.g. 22, 24) in the same head stack because the printed-wiring boards for the pre-amplifiers are layed out to accommodate two adjacent tracks per board. Tracks were selected from both head stacks to insure testing of the ability of the deskew electronics to handle differentials in the stack-to-stack spacing, which varies from machine to machine.

Group #2 consisted of tracks 5, 7, 30, 32, 57, and 59. This grouping was chosen to determine the ability of the deskew system to handle the 2-inch width of the head. The extreme edge tracks were avoided since it was felt that using these transports, which were not designed specifically for two-inch tape, caused errors due to edge damage to the tape. This problem would be avoided in a machine designed specifically for two-inch wide tape.

Group #3 consisted of tracks 33, 35, 37, 39, 41, and 43. These were chosen to be all adjacent in the same head stack to determine if transformer crosstalk in the head would degrade the BER.

In addition to the tests on the serial data stream, a large number of tests were performed on the individual tracks of group #1. As was stated earlier, this was done to investigate the reasons for the apparent wide variations in BER, observed during the debugging of the system.

In order to provide a sufficiently poor BER to make these differences observable, a tape of known poor quality was chosen to degrade overall performance from that observed using good tape. BER tests based on a 511-bit pseudo-random sequence revealed a differential on the order of one to two orders of magnitude, depending on

Speed	Transport	Group #1	Group #2	Group #3
120	1	1.6×10^{-6}	3.6×10^{-6}	2.7×10^{-6}
120	2	1.4×10^{-6}	5.1×10^{-6}	2.8×10^{-6}
7.5	1	3.0×10^{-6}	5.1×10^{-6}	4.6×10^{-6}
7.5	2	3.2×10^{-6}	3.1×10^{-6}	1.7×10^{-6}

Table 1. Bit Error Rate - Serial Stream (Low Burst)

Speed	Transport	Low Burst					
		1	2	3	4	5	6
120	1	8.3×10^{-6}	4.4×10^{-6}	9.5×10^{-6}	1.5×10^{-5}	4.3×10^{-6}	3.6×10^{-6}
120	2	4.4×10^{-6}	7.3×10^{-6}	5.6×10^{-6}	9.7×10^{-6}	4.7×10^{-6}	3.4×10^{-6}
7.5	1	3.8×10^{-5}	2.9×10^{-7}	2.4×10^{-5}	3.4×10^{-5}	2.7×10^{-5}	1.1×10^{-3}
7.5	2	2.8×10^{-5}	3.4×10^{-4}	4.7×10^{-4}	5.5×10^{-5}	1.6×10^{-5}	1.4×10^{-5}
Speed	Transport	High Burst					
		1	2	3	4	5	6
120	1	5.3×10^{-4}	3.8×10^{-4}	4.1×10^{-4}	1.3×10^{-3}	6.2×10^{-4}	2.8×10^{-4}
120	2	4.6×10^{-4}	3.2×10^{-4}	2.8×10^{-4}	4.1×10^{-4}	5.3×10^{-4}	2.7×10^{-4}
7.5	1	1.5×10^{-6}	7.8×10^{-7}	3.9×10^{-3}	5.9×10^{-3}	2.6×10^{-3}	5.3×10^{-4}
7.5	2	3.8×10^{-8}	1.4×10^{-7}	1.2×10^{-3}	4.8×10^{-4}	3.2×10^{-3}	1.6×10^{-3}

Table 2. Bit Error Rate per Track Without Deskew (Poor Tape)

Speed	Transport	Low Burst				
		1	2	3	4	5
120	1	8.2×10^{-6}	4.9×10^{-6}	1.0×10^{-5}	2.3×10^{-5}	1.4×10^{-5}
120	2	5.0×10^{-6}	6.6×10^{-6}	6.8×10^{-6}	1.1×10^{-5}	6.0×10^{-6}
7.5	1	4.0×10^{-5}	2.2×10^{-5}	3.9×10^{-5}	4.9×10^{-5}	7.2×10^{-5}
7.5	2	2.0×10^{-5}	3.9×10^{-5}	5.0×10^{-5}	8.4×10^{-5}	7.5×10^{-6}
Speed	Transport	High Burst				
		1	2	3	4	5
120	1	4.8×10^{-4}	5.1×10^{-4}	6.9×10^{-4}	5.5×10^{-4}	5.1×10^{-4}
120	2	3.4×10^{-4}	3.4×10^{-4}	3.2×10^{-4}	2.7×10^{-4}	3.7×10^{-4}
7.5	1	4.2×10^{-3}	1.5×10^{-3}	3.0×10^{-3}	1.3×10^{-3}	1.7×10^{-3}
7.5	2	1.9×10^{-3}	1.3×10^{-3}	1.2×10^{-3}	1.8×10^{-3}	2.0×10^{-3}

Table 3. Bit Error Rate per Track With Deskew (Poor Tape)

Speed	Transport	Low Burst		High Burst	
		Pass #1	Pass #2	Pass #1	Pass #2
120	1	6.0×10^{-6}	6.4×10^{-6}	9.5×10^{-5}	1.3×10^{-4}
120	2	6.2×10^{-6}	6.8×10^{-6}	8.6×10^{-5}	8.7×10^{-5}
7.5	1	1.7×10^{-5}		1.3×10^{-4}	
7.5	2	1.2×10^{-5}		7.8×10^{-5}	

Table 4. Bit Error Rate - Serial Stream (Poor Tape)

the mode of operation of the test equipment. The resulting data are tabulated in tables 2 through 4 and the reasons are discussed in Part 8.0 of this report.

8.0 ANALYSES OF TEST RESULTS

The reduction of packing density from 33 Kb/in as a goal to 30 Kb/in in practice resulted in a per-track bit rate of 10% and thus a serial bit rate potential of 10% lower than the goal of 240 Mb/s if 64 track heads are used. In order to meet an error rate near the goal of 10^{-6} , this reduction appeared to be necessary, as discussed in Part 5.0 of this report. It is noted that the initial program goal was limited to a density between 25 and 28 Kb/in, however (Sec. 1.2).

As has been stated earlier, some interesting insights into the problem of measuring bit error rates under various conditions were derived from testing individual tracks, with poor tape. These tests were initiated as a result of what was considered as an un-explainable wide variation in data rate as a function of test techniques during the debugging phase of the program. One of the major benefits resulting from the study was a greater understanding of the effects of various test techniques on BER performance. It is the purpose of this part of the report to discuss the inter-relationship between the various methods of testing and the measured error rates.

In systems which are band-limited in the sense that they either lack dc response, or have insufficient high frequency response to pass digital information without inter-symbol interference, or suffer from both failings, the BER often depends on the particular test pattern used during the measurement. The variation of the error rate as a function of the pattern chosen for the test is a measure of the pattern sensitivity of a given code. The subject of relative pattern sensitivities of various codes was studied extensively on a previous program (Ref. 2), and is covered in summary in Part 4.0 of this report, and Appendix A. Further details on this subject can be obtained from the above cited reference.

The variations in BER observed during de-bugging could not be attributed to pattern sensitivity problems since the same pattern, namely a given 511-bit pseudo-random sequence, was used for all tests. Even under these conditions, it became apparent that extreme variations of BER could be observed as a function of the test equipment used or the mode in which this equipment was operated, or both. These variations were investigated during the course of this program and which will be reported on here. However, in order to understand the reasons behind these wide variations it is necessary to understand the basic designs used in the various test equipments.

We therefore now turn to that subject.

8.1 Commercial Test Equipment

The standard measurement technique used for BER tests in systems of this type uses a pseudo-random sequence generator and a receiver/comparator. The generator generates a pseudo-random sequence consisting of a 511-bit word. The receiver has provision for generating an identical sequence and comparing this sequence on a bit-by-bit basis with the signal recovered from the recorded tape. For each error that occurs, a pulse is generated and drives a counter. In this manner the number of errors occurring over a period of time can be measured. From the knowledge of the total number of bits received and the number of errors, the BER can be calculated. Since it is necessary to synchronize the sequence generated in the receiver with the corresponding sequence recovered from tape, and since the method of synchronization varies depending on the test equipment used, or the mode in which this equipment is operated, or both, the actual BER measured may vary as a function of these parameters. For reasons which will be discussed, this implies also that the BER measured by any given test method may differ significantly from that achievable in the actual ultimate system application.

One of the test equipments most commonly used in the industry for these measurements is the Datapulse Model 213A. This device can be used interchangeably as either a data generator or a data receiver/comparator. The generator consists of a shift register with feedback taps. Up to ten stages of the register can be used. The outputs of any two registers is fed through an exclusive OR (XOR) gate back to the input. To generate a 511-bit pseudo-random sequence, nine registers are used and the outputs of registers 5 and 9 are combined through the XOR gate and fed back to the input (Ref. 4). A simplified schematic of a 63-bit generator when used in this mode is shown in Fig. 15a.

When used as a data receiver/comparator the unit consists of an identical generator, using the same feedback taps, with provision for synchronizing its sequence with the incoming data. Its simplified schematic is shown in Fig. 15b. In practice the operator has two options regarding the use of the synchronization switch shown in Figure 15b.

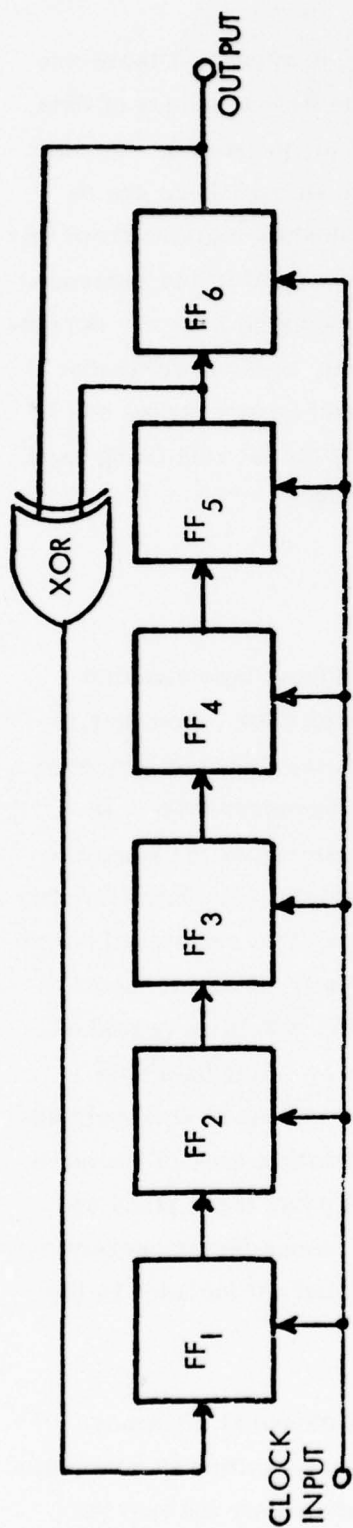


Figure 15a. Generator

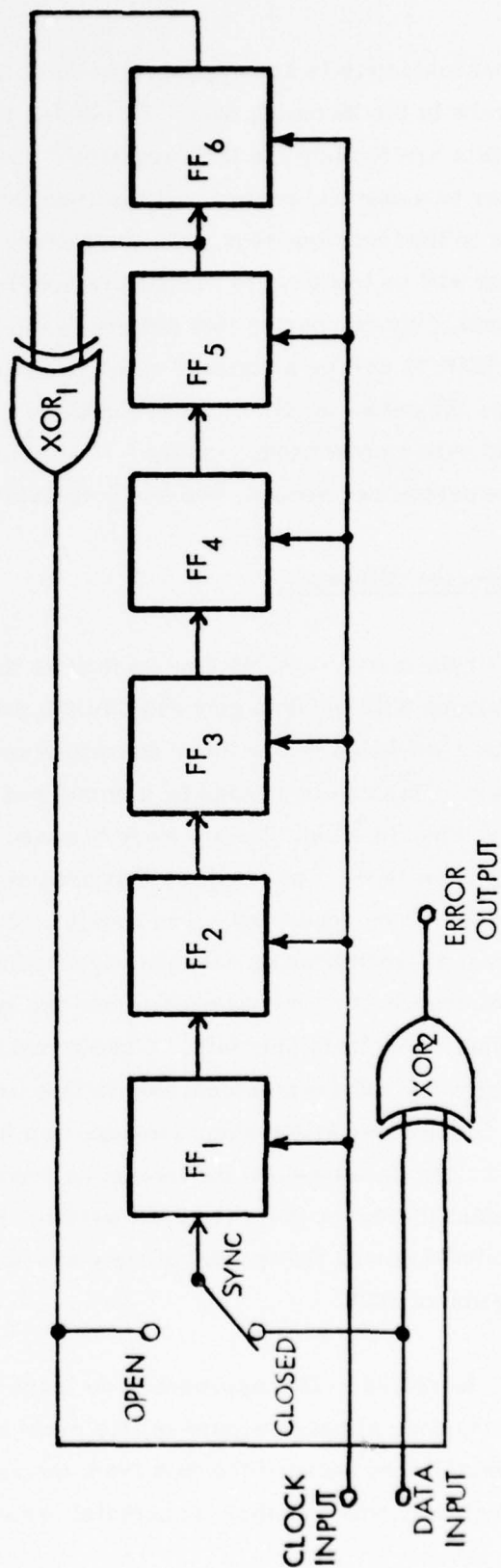


Figure 15b. Receiver/Comparator.

Figure 15. Sequence Generator for 63-bit Pseudo-Random Sequence

Synchronization is accomplished in the following manner: Assume that there are no errors in the incoming data. By closing the switch for the first nine bits of data, these bits are fed into the shift register. This is equivalent to "presetting" the shift register to a specific content. If the sync switch is now opened, and there are no errors in the incoming sequence, the pattern generated by the shift register from that point on will be identical to the pattern generated in the data generator and recovered from tape. By comparing this pattern to the pattern from tape using XOR #2, the output of XOR #2 will be a logical "zero" if no errors occur. For each bit error that occurs, the output of XOR #2 will change to a logical "one" and these changes can be counted with an electronic counter. Then with a knowledge of the bit rate being used and the errors per second, one can calculate the bit error rate.

8.2 Sequence Slippage

All of the above remains true so long as the data sequence from tape remains synchronous with the data generated in the data receiver/comparator. However, there is a condition where the synchronous condition can be lost, known as sequence slippage. This can be caused by a number of factors, to be discussed later. It happens when, in effect, one or more bits are added to or deleted from the sequence coming from tape. Once sequence synchronization has been lost a very large number of errors will be generated. The result is that these errors will be registered on the counter until such time as sequence synchronization is re-acquired. To re-acquire synchronization it is necessary to close the sync switch in Fig. 15b for a period of time equal to at least nine bits. When measuring BER on a system using a data generator and receiver/comparator in this mode, the number of errors accumulated on the counter due to sequence slippage is a function of the reaction time of the operator, i.e. the time between the instant he recognizes that a slip has taken place and the instant that he presses the sync switch. Because of this human factor, errors accumulated during that period of time are normally ignored and not included in the calculation of BER.

An alternative to this approach is to leave the sync switch closed at all times. When sequence slippage occurs in this mode of operation, re-acquisition is automatically established because the data from the recorder are continuously fed into the shift register, which is thus immediately reset to maintain synchronization.

There are two problems associated with this approach: In the case of isolated singular errors, the error is properly detected by XOR #2, but then the erroneous bit passes through the shift registers and two more errors are counted because the wrong information is fed back when this bit reaches register #5 and register #6. Thus singular errors are registered with a count of 3. The second problem is, that if there is a burst of 10 or 20 errors without sequence slippage, they cannot be distinguished from those errors caused by slippage. That is, when used in this mode, detection of sequence slippage is not possible. This is important since the detection of sequence slippage often aids one in isolating problems within a given system.

In any case, the error rate measured in the two different modes of operation may be significantly different depending on the mean error rate of the system and the system configuration.

All BER measurements made on this program and tabulated in tables 1 through 4 were performed with a different type of test equipment since the Datapulse 213A equipment described above is not capable of handling the serial data rates involved.

The test set used on this program consisted of a Tautron model MN-1 Pseudo-Random Generator and a Tautron Model MB-1 PCM Error Rate Measurement System Receiver. Operation of this equipment is the same as that just described with regard to pattern generation and error detection. It differs, however, in the manner in which sequence synchronization is established. It does not utilize a manual sync switch for obtaining sequence sync. There is, however, internal to the equipment, the equivalent in the form of an automatic switch. For initial synchronization, the "switch" is closed. The BER is monitored within the equipment, in addition to being displayed for the operator.

There are two options of operation. One option is known as the "Low-Burst Mode" and the other as the "High-Burst Mode". In the "Low-Burst Mode", once synchronization has been established, the "switch" is opened and the equipment operates in a manner identical to that described for the Datapulse unit with its switch open. The internal monitoring system then monitors the errors and if in any string of 100 data bits, 20 or more are in error, the system assumes that sequence synchronization is lost, classifies this as a burst, lights an LED indicator on the front panel to indicate that a burst has taken place, and "closes the switch" for a sufficient length of time to re-establish

synchronization. It then continues to detect errors in the normal manner.

The second mode of operation, classified as the "High Burst Mode", is identical except that the criteria for a burst error (or loss of sequence synchronization) is 20,000 bits in error out of 100,000 bits of data as opposed to 20 out of 100 for the "Low-Burst Mode". The desired mode of operation is selectable on the front panel via a toggle switch. Errors resulting from sequence slippage, can therefore vary during this "burst" by as much as a thousand to one depending on the mode of operation.

Thus, if one considers both types of test equipment, each with two modes of operation, a wide variation in measured BER can result depending on the actual BER of the system under test and what percentage of these errors are due to sequence slippage.

8.3 Reasons for Sequence Slippage

Up to this point we have discussed the results of sequence slippage. Let us now turn to the causes of sequence slippage: When measuring BER on a single track where the data have not been framed in any manner within the system, the predominate cause of sequence slippage is the so-called bit-slippage in the bit synchronizer. Bit slippage in this case is defined as the slippage of the clock generated by the VCO in the bit synchronizer relative to the bit stream entering the bit synchronizer from the recorder. This slippage is an integral number of cycles of clock. When this happens, one or more bits are effectively added to or deleted from the sequence and sequence synchronization is lost. All bit synchronizers will slip under certain conditions. This can be caused by the same parameters which effect BER, i.e. noise, tape drop-outs, intersymbol interference, timebase error, etc.

Mathematical analyses of the probability of bit slippage has been accomplished by others (Ref. 5). However, the mathematical treatment is extremely complex, and it is not useful in obtaining practical results on real hardware of the type used in high density digital recording. For this reason, the best approach for obtaining statistics on the probability of bit slippage is through the use of measurements on an actual recorder/reproducer system. If such measurements are to be meaningful, they should be done on a large number of channels taking into consideration the variations in heads, transport flutter, packing density, environmental conditions, tape, etc.

Furthermore, care must be taken to assure that a sufficient sample size be taken to result in meaningful statistical results.

Since, at the present time, the market requirements are so different from application to application, just which transport, track density, etc., should be chosen for such measurements is open to conjecture, and extensive measurements of this type could not be taken under this program.

At low packing densities, e.g. 16 Kb/in and 14 tracks/in, systems have been delivered which exhibited no bit errors whatever, on any of the 14 tracks, throughout the reel of tape. As packing densities and track densities are increased, we would expect an increased probability of bit slippage due to the same factors which cause an increase in the probability of bit error.

8.4 Other Factors Affecting Sequence Synchronization

Variation in measured BER between testing in the Low-Burst Mode and the High-Burst Mode on the system as tabulated in tables 2 through 4 can now be understood in the light of the preceding discussions even though they were limited to the problem of sequence slippage for data on a single track, where no multi-track framing of data takes place. Let us now turn to the problem of other potential causes of burst errors and the size of those bursts as a function the format of the data as recorded on tape.

In many applications the manufacturer of the recorder/reproducer equipment has no information about the detailed nature of the data except for the bit rate and the fact that the data are presented in NRZ-L form. However, the recorder is only a part of a larger system and the description of the format used in this system is seldom available to the manufacturer. Often the data are formatted to some extent: Data words are of a specific length, and blocks or frames consist of a specific number of these data words. In the total system, the lengths of these words and frames are well defined and suitable means for obtaining word and/or frame synchronization are provided.

In such cases, if the data can be suitably formatted on the tape, the number of errors due to loss of word or frame synchronization will depend on where in the word or frame the slip takes place. Loss of frame or word synchronization in such cases

is equivalent to what has been just described as loss of sequence synchronization. There is one important difference, however: If sync information, is provided in addition to the data, to make the frames or words, then re-acquisition of frame or word sync takes place automatically, at the moment this sync information is recognized. The actual number of errors that will take place under such circumstances depends on the position in the word or frame and where the synchronization loss occurs relative to the sync information.

As an example, let us consider the case where no word sync is used, but a frame sync is available and the frame length is 256 bits including a 16-bit sync word in each frame. Assume for the moment that no bit errors ever take place in the sync word and that frame synchronization is never lost as a result of a bit error in the sync word. Under these conditions, if there is a bit slip which occurs on the 200-th bit of a frame, there will be a 50% probability of bit error during the remaining 56 bits until such time as the sync word is detected and proper synchronization is re-established. Similarly under these conditions, assuming that no two bit slips occur closer than 256 bits from each other, the maximum number of errors that can occur due to such a condition is 256. If the data are random in nature, only about half of these will be counted as errors. Thus, 128 errors would be read by the test set-up used during this study. Furthermore, if there is an equal probability that the bit slip can occur on any given bit in the 256-bit frame, the slip, on the average, will result in a burst of 64 errors.

If we now turn to the problem of measuring BER on more sophisticated hardware, namely a system containing deskew electronics, we can discuss the problem of frame synchronization. In such a system the data are framed in 256-bit blocks prior to recording. Because of the arguments posed in the previous paragraph, the BER should approach that measured when a bit slip occurs and, indeed, it does. Under these conditions, it is not surprising that different BER's can be measured on the same track depending on whether or not the data is deskewed.

Up to this point we have assumed that loss of frame or word synchronization can take place only as a result of bit slippage. There are other ways in which loss of frame synchronization can occur, however.

Frame synchronization can be lost in the deskew electronics if the sync word is not

recognized due to a bit error in the sync word, and the data in that frame simultaneously contain any group of bits identical to the sync word.

The probability of this happening in any given system will affect the overall error rate of the system. Hill and Weblemoe (Ref. 6) have analyzed this problem and developed equations for calculating this probability, which is related to the length of the sync word, the particular pattern of the sync word, the length of the frame and the synchronization strategy used.

Independent of the work done under this contract, studies were made of the system used for deskewing the data and appropriate calculations were made to determine if the choice of sync word and the method of sync detection used would provide for a reasonably low probability of loss of frame synchronization and the burst errors caused by such a loss. The calculations revealed that, in the system used, there was significant room for improvement achievable by changing both the sync word and the method of detection.

Subsequent tests were run on a system to try and verify these calculations, but they were not verifiable. The measurements revealed that there was, in fact, a very low probability of loss of frame synchronization due to this cause. Once these measurements were made, some thought on the subject resulted in what appears to be a valid explanation of the reason for the inconsistency between the data and the calculations: As in all probability calculations, an interaction exists between the theory developed and the statistics involved in a real situation. For example, calculation of the probability of loss of frame synchronization due to the causes described in this section depends on the accuracy of assumptions made regarding the probability of bit error in the system. All of the theory developed assumes that there is an equal probability of bit error on each and every bit that passes through the system. This is true for non-bandlimited NRZ-L data in the presence of white gaussian noise. To assume that the same is true for the case of high-density digital recording where there is severe bandlimiting and the code used is the Miller code (which was used for the specific test being discussed) is erroneous.

In general, papers discussing the choice of sync word and the reliability of detection of sync words, assume that the probability of bit error is equal for all bits. Under such circumstances, it is common to recommend the use of Barker codes for sync

words. Barker-code chosen words have unique correlation properties which increase the probability of recognizing them when seen in the stream. However, once again, the probability calculations used to prove the superiority of Barker words under such circumstances are based on use of the NRZ-L code in a non-bandlimited system in the presence of noise.

In systems where: a) The signal is severely bandlimited; or b) The code is significantly different from NRZ-L (which both Miller code and the newer M^2 -codes are, since they are both Markov processes), the calculations are not valid. Furthermore, in such systems, suitable probability calculations are not mathematically tractable. Thus, the ultimate test is to determine the probabilities in question through the use of experimental data. As was stated before, such experimental data were gathered independent of this contract and revealed that the choice of sync word and sync detection scheme used in the system performed in such a manner as to indicate that if loss of frame sync occurred, it was more likely that it was due to loss of bit synchronization than due to lack of proper detection of the sync word.

Furthermore, since the sync word detected in the deskew logic used consists of 14 "ones" in a row, and the test method used on the 2-inch feasibility model consisted of a pseudo-random, 511-bit word, and such a word cannot, by definition, contain more than nine "ones" in a row, loss of frame synchronization due to bit errors in the sync word is highly improbable.

8.5 Additional Points

Finally, it should be made clear that in any real system as opposed to a system being tested for BER in the laboratory, the actual error rate observed may be either better or worse than that measured in the laboratory, depending on the way that the real data are formatted on tape. This formatting may be partially due to the framing within the recorders, such as in the deskew circuitry, or it may be due to the particular way in which the user's data are formatted prior to being delivered to the recorder.

As a minimum, it is important that these factors be understood at the system level, to assure that the specification imposed on the recorder manufacturer not be overly conservative or liberal for a particular real application, and that such specifications include specifics regarding the measurement and interpretation of bit-error rates as applicable to the overall system requirements.

9.0 CONCLUSIONS AND RECOMMENDATIONS

The study revealed that the recording and reproduction of a total throughput rate of 240 Mb/s should be feasible in the near future. It provided the necessary insight into several problem areas which need further work in order to develop such a system. This work is considered within the realm of current technology and does not require a major breakthrough in the state of the art. It further proved the feasibility of developing such hardware and maintaining the capability for "slow-down" (time-base expansion) on reproduce, and machine-to-machine compatibility.

The study helped to confirm the concept that more is to be gained in packing density per unit area of tape by increasing the track density than by increasing the packing density per track. This conclusion arises from the fact that on the basis of the data taken on this study in combination with that taken on a previous study (Ref. 2), and comparing the results with two different track densities at the same packing density per track, one can conclude that a decrease in track width of 10% (caused by an increase in the number of tracks per inch of 10%) will result in a degradation of record margin of about 1 dB, whereas a decrease in per track packing density of 10% will increase the record margin by about 2 dB. Thus, for the same packing density per square inch, a 10% increase in track density would increase the record margin by 1 dB.

Given that the same error rate was allowable in both cases, this extra dB in record margin should allow for an increase in density per square inch by an amount equal to about 5%.

These results should hold up to the point where track densities become so high as to cause problems with crosstalk. Previous experience with crosstalk problems indicates that they will first become apparent due to either transformer or capacitive crosstalk in the head, depending on the per-track bit rate. One method of relieving these problems would be to interleave three head stacks instead of two in order to achieve the increase in track density on tape and at the same time maintain adequate shielding between tracks in the head stack.

As track densities are increased even further, the next limiting factory would be tape crosstalk due to the problems related to tape tracking. These problems will place

some upper limit on the track density on tape, although clearly it was above that used in this study.

The study also pointed out the need for further work on the signal electronics if they are to be able to handle higher bit rates per track. In particular, work must be done on the head driver and the direct reproduce amplifier. However, this work is considered well within the state of the art.

Finally this study, plus other Ampex-related work, emphasized the difficulty of measuring the recorder's performance in terms of bit error rate. It is not, for example, enough to quote a BER on a repetitive 511-bit pseudo-random sequence. One must first decide whether "burst errors" should be included. Ideally one would like to separate those errors caused by tape defects from those caused by other system defects in order to determine if one recorder has significant advantages over another. A second variable is how the recorder handles bursts due to tape defects; it may, for example lose bit synchronization for a significant number of bits beyond a burst caused by tape defects alone. This introduces still another problem in that the operational use of the recorder is unlikely to be with 511-bit pseudo-random sequences. The optimum format to minimize burst length operationally and when testing with a pseudo-random sequence may call for substantially different solutions. This will be particularly true if pattern sensitivities exists in the system. Furthermore the length of a burst caused by a bit slip (which may be caused by a tape dropout) will depend on the resynchronization time which in turn will depend on the format used, and indeed this problem should possibly be a factor in choosing the operational format as well as the formats used within the recorder for other purposes, e.g. des-kew, error detection and correction etc.

Thus, apart from the easily defined target of increased density (either in bits/in or tracks/in), there are other areas that appear worth further study:

- a) Formatting techniques which decrease errors due to resynchronization times.
- b) Error detection and correction codes which are optimized for these types of recorders.
- c) Optimum methods for measuring BER in the tape recorders and how these methods are influenced by the format of the data to be recorded.

Such studies should result in both better recorders and improved methods for the evaluation of such recorders by both the government and the industry; thus assuring that test procedures used are capable of revealing potential weaknesses in the recorder in an operational environment in advance of hardware acceptance.

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APPENDIX A
Dependency of Bit Error Rate Measurements
in High Density Digital Recording
On Patterns used for Testing

In high density digital recording, some channel codes are extremely pattern sensitive. This comes about because of intersymbol-interference in a system due to a lack of insufficient bandwidth. In a recorder/reproducer at high packing densities where the bit rate being recorded is high relative to the bandwidth of the recorder, the use of different data patterns for testing can have a significant effect on intersymbol-interference and the resulting error rate.

Since the recorder does not have the capability to reproduce dc, codes which have a capability of a large dc offset as a result of particular patterns of logical "ones" and "zeroes" will exhibit poorer error rate performance when subjected to these types of patterns than when subjected to conventional pseudo-random patterns. It is not always easy to find that particular pattern among the infinite number available which will produce the worst-case condition for a particular code. For most common codes used in the industry however, the problem is simplified. For example, confronted with a code designed to block the data into an n -bit word, one would search for a particular n -bit word which, if repeated often enough, would cause a dc offset. If the code was designed to convert n -bit words into $n+m$ bits, one might search for both a variety of n -bit words and $n+m$ bit words which might cause the worst-case pattern to appear.

In Miller code, it has been known for some time that the worst case pattern is 011011011011011....etc., in the sense that this pattern causes the worst-case dc offset. This happens to be a 3-bit repeating word. In order to test for this condition and other possible ill-conditioned patterns, Ampex designed and built a specialized piece of test equipment. Among many others, it generates the above pattern, and repeats it a very large number of times.

The special unit used in our tests is called a "ramp generator" and is shown in simplified form in Fig. A-1. The 6-bit binary counter parallel-loads a 6-bit shift register which is clocked out serially. The divider in the clock is such that the 6-bit serial word can be repeatedly generated from 2 to 128 times, before the next 6-bit word is generated. The name "ramp generator" comes from the fact that if the output

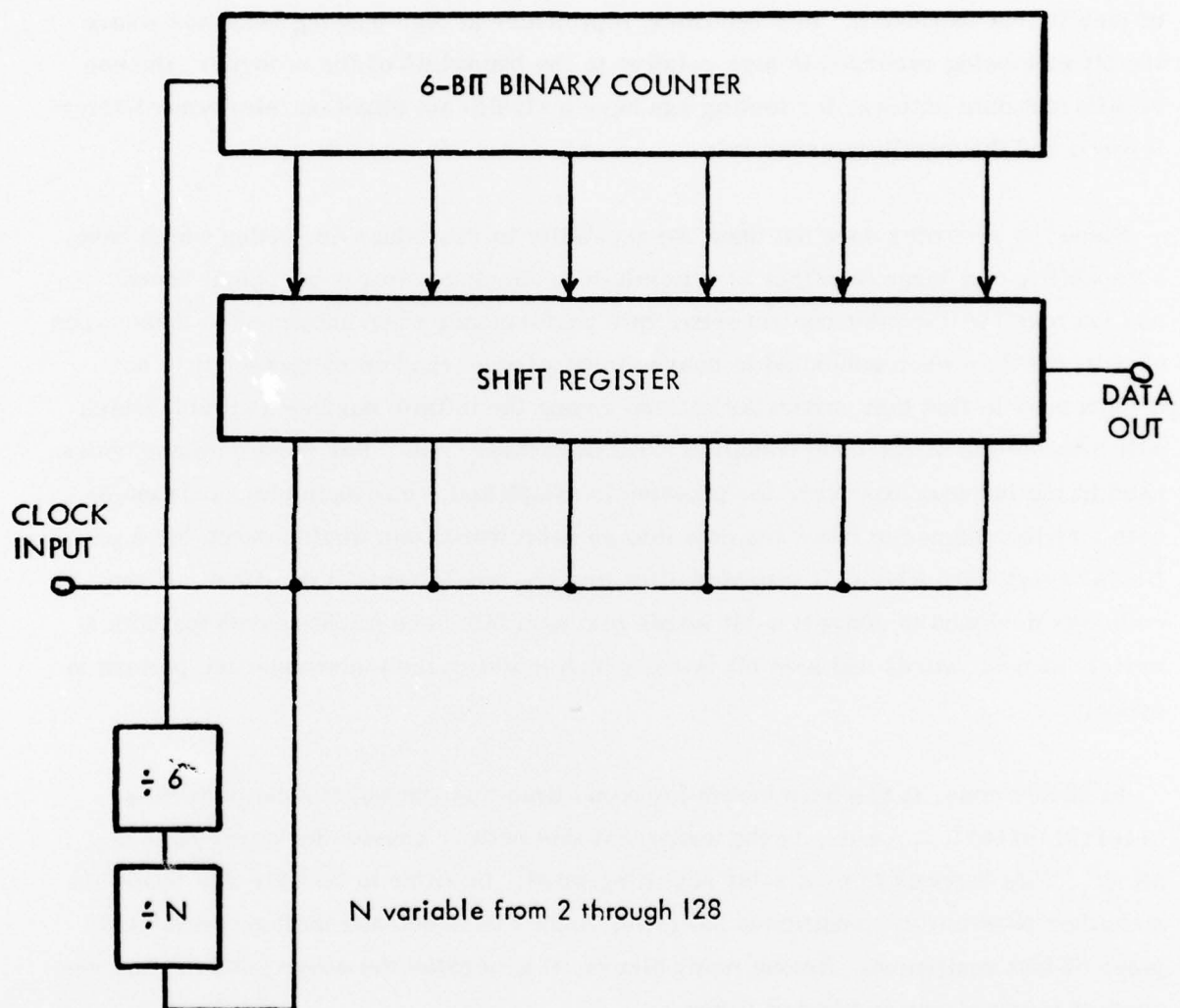


Figure A-1. Block Diagram of Ramp Generator

of the counter is fed to a Digital-to-Analog converter its output will be an analog ramp signal. At 3.6 Mb/s, if a 511 bit pseudo-random sequence is used as the test pattern, the lowest discrete line frequency present in the data waveform is a fundamental component of about 7 kHz, when the tape is reproduced at 120 in/s or around 440 Hz when it is reproduced at 7.5 in/s. When the ramp generator with a word repetition of 128 times is used, the lowest frequency component under the same conditions is about 70 Hz at 120 in/s reproduce speed, and 4.5 Hz at 7.5 in/s.

Detection of bit errors is achieved by using an identical ramp generator as a data comparator. Synchronization is accomplished by presetting the counter to the proper count whenever 12 zeroes in a row are seen in the incoming data.

We have found the ramp generator particularly useful in studying the relative pattern sensitivities of a variety of codes. In particular, measurement of the error rate by means of the ramp generator with various numbers of repetitions of the 6-bit word, and comparison of the results of these measurements against each other as well as against those obtained with pseudo-random sequences of various lengths, offers a measure of the pattern sensitivity of a number of codes. The choice of the number "6" for the length of the word came about as a result of experience with Miller Code and its worst-case pattern. The generator does indeed generate this worst-case pattern repeatedly over a long sequence of bits. Tests demonstrated that the patterns generated by this device proved the modified NRZ code to be rather pattern-sensitive. Greater pattern-sensitivity in this code might have been observed had the choice of the number of bits per word used in the ramp generator been "7", since a common implementation of this code operates in such a manner as to block the incoming data into 7-bit words, each of which are then converted into 8-bit words (Ref. 2).

Figures 11 through 14 in the body of this report illustrate the type of information which can be obtained about the relative pattern sensitivity of a code using this ramp generator. These figures were taken from Ref. 2 which contains a great deal more information on the problems of pattern sensitivity than can be included in this Appendix.

APPENDIX B

The Miller-Squared Code

Jerry Miller of Ampex, invented the Miller-Squared (M^2) code. The description of the M^2 code is simplified if it is described as a modification to the Miller code. Therefore, the Miller code will be described first.

The Miller Code

The encoding rules for Miller code are as follows:

- a. A logical one is represented by a transition at the center of a bit cell.
- b. A logical zero is represented by a transition at the leading edge of the bit cell, unless preceded by a logical one, in which case this transition is suppressed.

Figure B-1 (a) represents a data stream encoded in the Miller Code.

The dc content of a repetitive signal is represented by the equation

$$dc = \frac{1}{T} \int_0^T f(t) dt$$

Figure B-1 (b) is a plot of $\int f(t) dt$. This plot is also called the digital sum variation (DSV). The dc content is proportional to the rate of growth of this DSV. As can be seen by comparing Fig. B-1 (a) with Fig. B-1 (b), the pattern which creates the maximum rate of growth of the DSV is a repetitive pattern of 0110110110 It is this pattern in the Miller code which is worst case in the sense that it has the largest dc content.

The M^2 Code

The M^2 code is a code which is similar to the Miller code but with additional rules. All possible binary patterns can be classified as being made up of patterns falling into one of the following classes:

- | | |
|---------|--|
| Class A | 1, 11, 111, |
| | i. e. any number of logical ones in a row |
| Class B | 00, 010, 01110, |
| | i. e. a pair of zeros or a pair of zeros separated by an odd number of ones. |
| Class C | 0110, 011110, |
| | i. e. a pair of zeros separated by an even number of ones. |

When the binary data is encoded into Miller code, the dc average of the resulting signal will be zero if the pattern belongs to either Class A or Class B, but will be finite if the pattern belongs to Class C. This can be seen in Fig. B-3 where the various classes of waveforms are sketched.

To encode in M^2 code the rules are as follows:

- a. If the data pattern falls into Class A or B encode by the rules of Miller code.
- b. If the data pattern falls into class C, encode by the rules of Miller code except suppress the transition normally used for the last logical one in the pattern and classify the next pattern starting with the zero following the suppressed transition.

Figure B-2 illustrates the same binary pattern used in Fig. B-1 encoded into M^2 code with the suppressed transitions indicated by an "x" over the binary one. The integral of the resulting waveform i. e. the DSV, is also plotted in the figure. As can be seen, this DSV is bounded, with the bounds being represented by dotted lines. It is these bounds which make the code dc free. As an aid to understanding, Fig. B-4 illustrates the classifications of the various patterns occurring in the binary data used as an example for an M^2 encoding system.

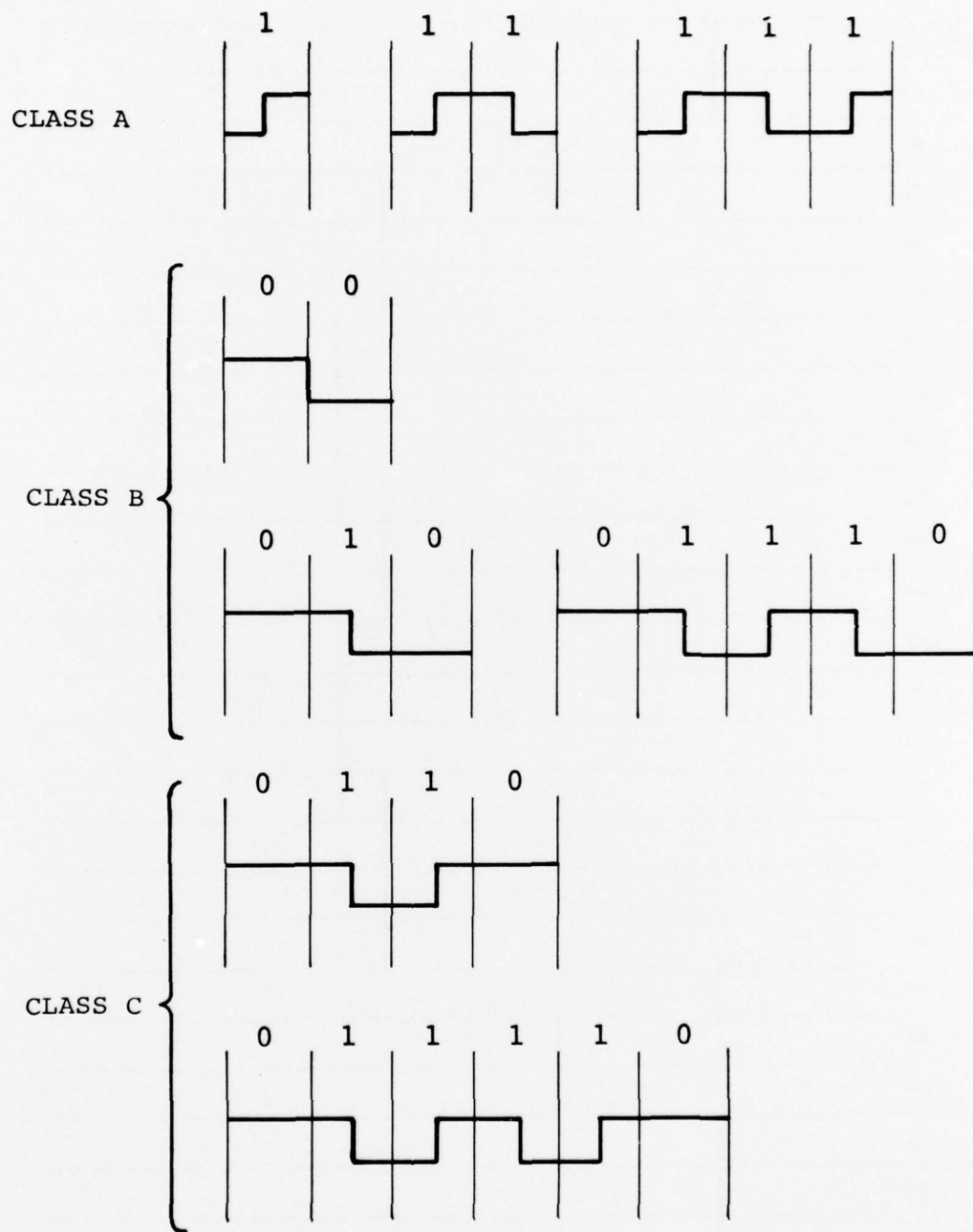


Figure B-3. Sketch of Waveforms by Class

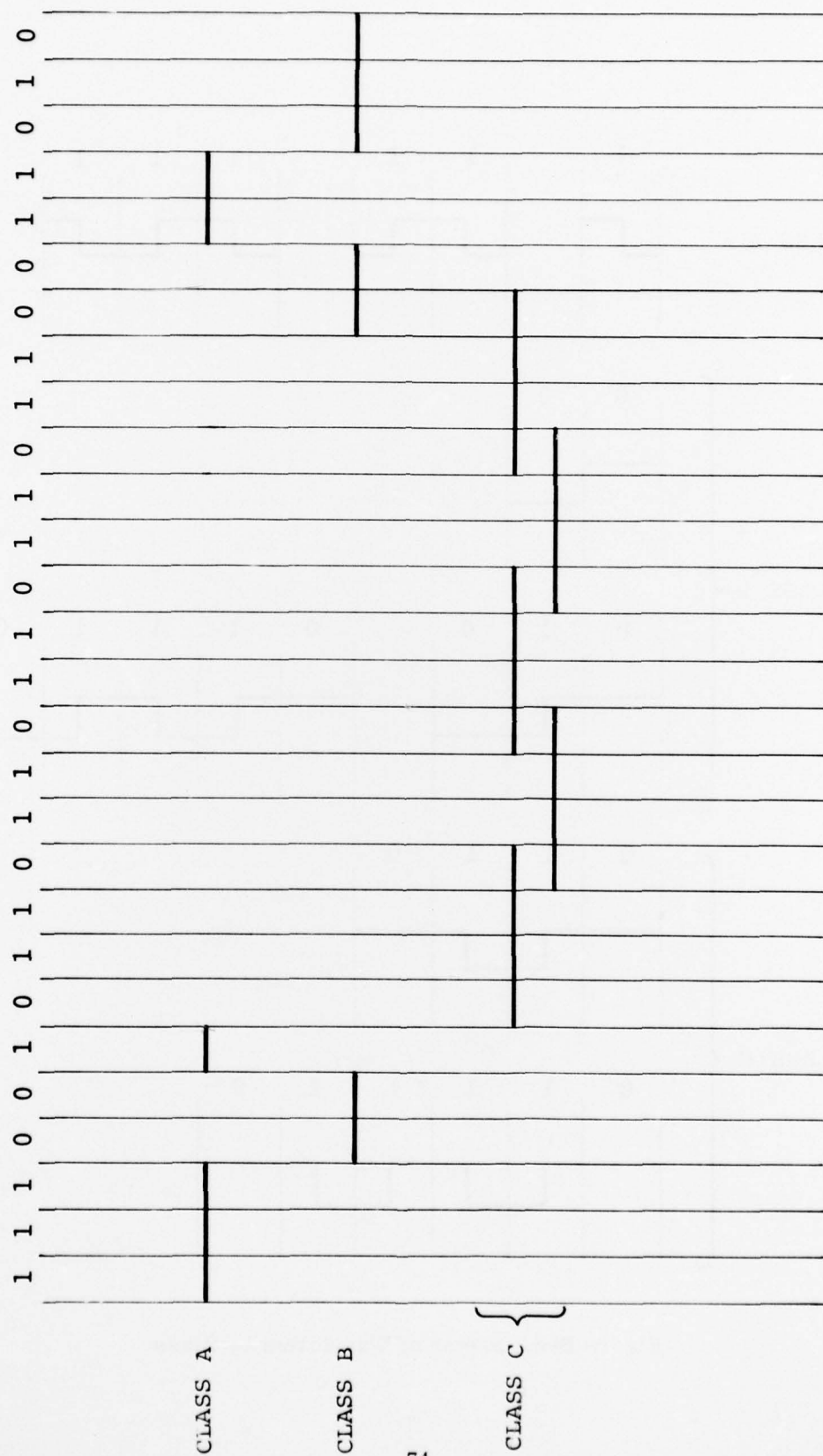


Figure B-4. Pattern Classifications

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